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SCENET roadmap for superconductor digital electronics

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Abstract

The roadmap gives an overview on status and future developments in Superconducting Digital Electronics (SDE). Key areas in SDE under focus are applications, circuit simulation and design, circuit fabrication, interfacing and testing, cooling and system aspects, and new devices and materials. Care was taken to establish the vital link between research and development on the one hand and the industrial view on the other hand. The present roadmap is based on extensive input from the roadmap working group on SDE established by *SCENET – the European Network for Superconductivity*, intensified by the activities of the *FLUXONICS Network – the European Foundry for Superconducting Electronics*. It is the result of many years of discussion in the group and of consultations with experts in the field, on the way to bring together industrial expectations and visionary extrapolation and current status of technology.

Foreword

After an enormous activity of fundamental research in superconducting materials, time has come to exploit the unique properties of these materials for industrial applications. So, after the "decade of the materials science" it is now the turn of the "decade of the market". In this respect, the European Commission supports a network, called SCENET, dedicated to single out these applications. The objective of the SCENET network is to bring together academic and industrial groups, to transfer knowledge from academic institutions to industry and to promote new ideas for innovative research projects. The network activities are chosen in line with a vision of potential industrial applications. Therefore the European Commission has specifically asked for a technological roadmap indicating the research needs in superconductivity for industrial applications and in particular on electronics. Several working groups have been set up for this purpose, one of them investigating superconducting digital electronics.

A roadmap is an extended look at the future. Any document of this kind starts with a careful analysis of the state of the art, stating the progress made in the past and analyzing the remaining technological difficulties for applications. Discoveries leading to scientific breakthroughs cannot be predicted, but scientific and technological development can be accelerated if you know exactly what you are looking for. And this is the task of this roadmap for superconducting digital electronics, i.e. starting from possible industrial applications to derive to quantitative figures on the technological specifications. A roadmap in the European perspective

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should point to the strengths and opportunities in the European R&D and markets which give different weight to military versus commercial, to computers and communication switches versus digital signal processing and calibration in the US and Japan versus Europe. Therefore, some roads could turn out to be more important or used differently in different regions of the triad.

The market determines what are suitable applications and its size is an indication for potential resources to be allocated. Unfortunately the market is difficult to predict and changes in the consumer behaviors may have a drastic consequences for research. Up to now the main driver for electronics has been computing and in particular PCs. However, it may perfectly be that in the future, telecommunications will be in the driving seat and new opportunities may appear for low and high temperature superconducting electronics. One example: Assume that it would be possible to build an A/D converter with a working temperature of about 40 K be packaged together with HTS-receive-filters suitable for a base station for mobile telephony. Currently the number of mobile telephony users in 2000 is nearly 500 million and it will double by the year 2003. As one base station serves about 1000 users, the base station market over the next three years will be in the order of 1 million, including replacement of old base stations. If we assume further that 10% of all future base stations by year 2003 will be equipped with front-ends with one HTS-A/D converter plus HTS-filter per sector, then the market would be in the order of 33.000 units per year. As the manufacturing price must be comparable or lower than conventional base stations, i.e. maximal 10.000 €/unit, the annual market is in the order of 330 M€ (no such weight to very low integrated, low yield, low reliable, HTS A/D converters, which become very expensive if they cannot be reliably made and delivered in systems which give customers satisfaction).

This example shows that development in superconducting electronics and market considerations cannot be separated. Therefore the objective this roadmap is twofold, to give precise specifications for superconducting technology to be competitive to enter into the market and to detect new applications with current or future technology.

The working group has identified five key areas, namely circuit design and simulation, circuit realization, interfacing, cooling and system aspects and testing. Each of these areas is vital for the development of industrial applications and will be discussed in more detail in the following.

Let me remark that this roadmap is not the view of individual persons, but the consensus view of the senior researchers of the main European laboratories. It does not pretend to be complete or to be the only possible visionary extrapolation. On the contrary it is intended to be a *dynamic* document is to be updated periodically in function of the technological progress and the market pull. This is also an *open* document inviting any person to put forward his or her view in order to aim at a complete picture of the field and to be used as a neutral guideline for decision makers in research, industry or government.

Ramón Compañó
European Commission
Directorate General Information Society

1. Introduction

Superconductor digital electronics is currently the fastest densely integratable electronics available with excellent potential for future ultra-fast data processing. The most successful realization of SDE is the Rapid Single Flux Quantum (RSFQ) logic, developed originally by Likharev and co-workers. Quite complex circuits have been realized in low-T_c superconductivity, circuits of low complexity have been demonstrated also in high-T_c superconductivity.

Compared to the huge research and development effort in semiconductor electronics, only a tiny amount of funding and research effort has been put into superconducting electronics. Nevertheless, the achieved results demonstrate the feasibility from basic building blocks for digital applications to digital processors, analogue-to-digital- and digital-to-analogue converters. The most outstanding properties of this technology are its extremely small energy consumption and its pico-second range switching speed at typical feature sizes in the micrometer range. These properties can help to overcome limitations in the application of semiconductor devices: for applications in which very high processing speed at low power consumption or very high resolution or a natural gauge such as the flux quantum is required or any combinations of these, superconducting electronics is unique. No other technology currently available or visible at the horizon of current technology development can deliver these unique properties. However, superconductor electronics is not intended to replace general purpose semiconductor electronics but to provide special purpose high end solutions and digital signal processing that are unaccessible for semiconductor electronics. This advantage already has been demonstrated.

In order to make a compact overview over status and future developments in superconducting electronics available to interested parties such as electronic industries and research institutions, the steering committee of the European Network of Excellence on Superconductivity (SCENET) decided during a workshop in Ravello/Italy (October 28–31, 1998), to establish working groups with the task to develop roadmaps and action plans for superconducting electronics. In this context, a working group on Superconducting Digital Electronics was established with H. Rogalla as chairman. The group consists of representatives of the field. The general procedure and its time frame are specified in the "SDE Working Plan".

The working group identified the following key areas in SDE:

- Circuit design and simulation
- Circuit realization in low-T_c and high-T_c
- Interfacing

- Cooling and system aspects
- Testing

In addition care was taken to establish the vital link between research and development on the one hand and the industrial view on the other hand. This link is being intensified by the increasing activities of the FLUXONICS network.

The present roadmap is the result of many years of discussion in the group and of consultations with experts in the field. On the basis of foregoing Versions V.1.4 (March 2000) and V.2.2 (November 2001), the present Version V2.3 (July 2005) has been completed under strong engagement of the members of the roadmap working group on SDE. It is certainly still not complete and needs further improvement; it is a third step on the way to bring together industrial expectations and visionary extrapolation and current status of technology.

2. Applications

2.1. Industrial aspects

All present applications of superconductor digital electronics (SDE) are performance rather than cost–benefit driven. This makes it hard for SDE to penetrate e.g. the huge telecommunications market, since there are few technology bottlenecks yet perceived by industry, which conventional (semiconductor or integrated optical) technologies are expected to resolve in the near future. The common belief in Moore's law is certainly the worst enemy of SDE in the short run. Special purpose superconductor electronics with its cooling requirements to liquid Helium temperature is not intended ever to replace general purpose semiconductor electronics but to provide special purpose high end solutions and digital signal processing that are unaccessible for semiconductor electronics. In regard of such high end solutions and digital signal processors it would pay not to try against heavy obstacles Moores law is facing but to make use of moderately integrated Niobium technology instead to get the same result more reliably at a much lower power level and smaller over all dimensions.

In the longer (more than 5 year) perspective the cost–benefit side is brighter for SDE, as serious problems are looming on the horizon for high-speed semiconductor technology. The fabrication costs for semiconductor (deep submicron) downscaling are increasing so rapidly with each new generation (mainly due to the interconnect problem), and the costs for chip cooling are increasing so dramatically with downscaling, that the comparatively simple and robust niobium technology may soon prove to be cost-advantageous—even taking its "cooling penalty" into account. Although deep-cooling semiconductor circuits (to an optimum temperature of around 100 K) will undoubtedly shift the Moore curve, and prolong its life somewhat, the niobium based RSFQ technology is presently the only mature, low power, ultra-high speed technology alternative in the long run. RSFQ electronics offer circuit speeds of the order of 100 GHz at more than three orders of magnitude lower power dissipation than semiconductor circuits—and without the performance deteriorating interconnect problems of the semiconductors!

Consequently, it is very important for European competitiveness that a readiness for an industrial demand, within 5–10 years from now for RSFQ technology, is built up. There are virtually no such resources for industry to tap or recruit from today. With a world class RSFQ capability maintained until the day that this cross-over point comes, Europe would be ready to participate in this high end race, otherwise not. Key persons in the field need sustained support and key technologies, not hitherto paid much attention to in academia, such as cryo-coolers, cryo-packaging and interfacing of RSFQ chips to semiconductor circuitry, need to be developed. Also, and of utmost urgency, is that European foundries for Nb and NbN process technology are established and made open to an all-European effort towards a sub-micron RSFQ chip technology.

2.2. Applications—Market outlook

In Europe, there is successful research going on on RSFQ but no market is to be seen up to now. Research and marketing of RSFQ should focus on some highlights with European strength that is e.g. on quantum calibration (voltage standard) where RSFQ circuits of moderate integration could improve and boost such circuits in price, handling advantage, and usefulness for the customer. A hybrid chip or even an integrated circuit could replace bulky and costly microwave equipment.

RSFQ-circuits are ideal partners to analogue superconducting quantum electronics circuits thus adding adapted, very fast digital signal processing to devices like SQUIDs and the new superconducting quantum interference filters (SQIFs) for high frequency applications. The application field of ultra sensitive electromagnetic detection has ever since been dominated by superconducting quantum electronics in the most ambitious basic investigations in physics. The time has come that the applications cover national security and integrity. And these will be important markets.

On the long run RSFQ circuits are expected to be the ideal readout and operation circuits for superconducting quantum computers, a field which can be considered as a European stronghold. Cooling to liquid Helium temperatures in such cases can be tolerated since the quantum performance needs such cooling anyway.

Table 1 contains a *list of possible applications* of superconductor digital circuits. The "junction count" is a measure of the complexity of the circuits—an order of magnitude estimate of the number of junctions required for the circuit, and, hence, an indication of the maturity of the technology required for their realization. The *market size* estimates are simply the best "educated guesses" that can be made at present.

Table 1
Possible applications of superconductor digital circuits

Application	Junction count	Market size
Integrated SIS receivers with correlator	10^6	Small
Digital multichannel SQUID arrays	10^5	Medium
DC voltage standards	10^4	Small
AC voltage standards, digital synthesiser	10^5	Medium
A/D converters	10^4	Large
D/A converters	10^3	Medium
Dc/ac quantum voltmeters	10^5	Large
Time-digital converters	10^3	Medium
Digital SFQ test circuits for rf metrology	10^3	Medium
Coding/decoding systems for secure communications	10^3	Medium
Frequency dividers, digital frequency meters	500	Medium
Transient recorders	10^4	Medium
Samplers	10	Medium
Digital beam forming microwave antennas	?	??
Read-out for multipixel focal plane array imagers	?	??
TeraFLOPS workstation	10^6	Medium
PetaFLOPS computer	1000×10^6	??

2.3. Comments on the prospective, commercially important applications

2.3.1. Mobile radio communication

Mobile radio communication, either in the form of the "third generation" wideband CDMA or multistandard, software defined radio (SDR), presently offers very promising applications for SDE. The most serious bottleneck here is the A/D converter, which, ideally, should have a Nyquist frequency of 120 MHz and a signal-to-noise ratio (SNR) of 14–16 (effective) bit precision. No such semiconductor A/D converter yet exists or is expected to exist within the next 5–10 years. (According to a recent survey by R. Walden, Hughes Research Laboratories, the improvement in A/D converters has so far been only 1 bit every 8 years!) Niobium-based superconductor A/D converter chips, however, even in their present highly non-optimized design and coarse 3.5 μm technology, clearly exhibit this performance potential. With a very modest investment in circuit optimization and Nb-chip fabrication technology they should be right on target.

RADARs tend to use digital data processing as much as possible: High resolution ADCs with 10–100 MHz bandwidth are required in the architecture of digital receivers. Their present performance limit their use in digital RADARs to a few thousand per year. This figure could be increased by approx. a factor 10 using superconducting ADCs, with 14–16 bits resolution. They have many common features with the ADCs required for the Software Defined Radio.

Wide Band RADARs for digital spectrum analysis need high speed ADCs with performances only achievable with the HTS technology (*about 10 bits at 4 GHz, or 8 bits at 8 GHz*). This is not only due to the small aperture time of the Josephson junction, but also because the issue of clock jitter is less critical for both Σ–Δ and flash type superconducting ADCs than for their semiconductor counterparts. Presumably, wide band spectrum analysis and digital receivers for telecommunications constitute comparable market sizes for superconducting ADCs.

Other prospective RSFQ applications are for digital signal processors (DSPs), for advanced coding/decoding and fast Fourier transformation in real time, for future multimedia mobile communication and radar systems.

2.3.2. Metrology and lab instruments

Metrology and lab instruments, based on the exact Josephson voltage-to-frequency conversion, such as voltage standards and sampling oscilloscopes, are established SDE applications. (In 1987, Hypres Inc. introduced a 70 GHz sampling oscilloscope and Time Domain Reflectometer based on a superconducting sampler, but the market penetration was not sufficient to sustain production—about 20 instruments sold by 1990.) Voltage standards including programmable voltage standards, pseudo-random noise generators and HF noise power level detectors are examples of SCE circuitry that could increase the market segment.

Programmable voltage standards of fundamental accuracy have been realized with binary sequences of non-hysteretic junctions [1]. Fig. 1 shows the photograph of a 10 V Josephson series array chip for a programmable voltage standard and the appropriate current–voltage characteristics under circuit operation. At PTB Braunschweig, in SINIS (superconductor/insulator/normal metal/insulator/superconductor) technology, a high grade of circuit complexity was achieved by integrating up to 70,000 large area junctions ($8 \times 50\ \mu m^2$) for application in voltage standard circuits. A 10 V constant voltage step was reached under 70 GHz microwaves irradiation less than 1 mW. The power level is much lower, and the voltage step width of up to 200 μA is much larger than for conventional SIS arrays. The critical current density is $J_c = 188\ A/cm^2$ at $I_c = 0.75$ mA and $V_c \approx 150\ \mu V$. The applied 70 GHz microwave could be homogeneously propagated by coherently coupling the Josephson oscillations of all junctions distributed over 64 parallel microwave parts. The number of junctions' failure due to shorts is clearly less frequent than for SIS (superconductor/insulator/superconductor) based circuits. To phase-lock the coherent oscillator system to an external microwave source, only a small amount of microwave power is to be provided by the external oscillator.

A new microwave circuit for Josephson voltage standards was developed at the IPHT Jena. In these circuits coplanar strips (CPS) are used instead of microstriplines for the integration of the Josephson junctions into a microwave transmission line. Compared to microstripline circuits the CPS design duplicates the scale of integration and simplifies the fabrication technology. Fig. 2 shows a

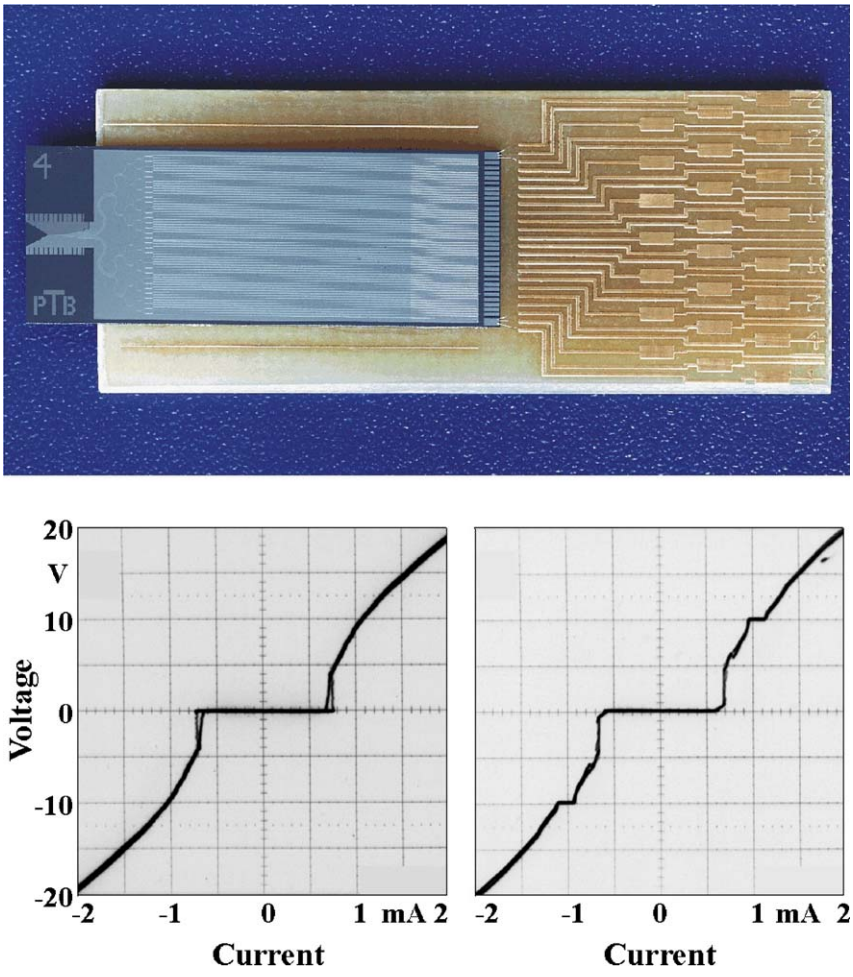


Fig. 1. Ten volts Josephson series array consisting of 69,120 SINIS junctions, upper: photograph, chip size: 28.0 mm × 10.5 mm, lower: current–voltage characteristics, left: without microwave irradiation, right: under 70 GHz microwave irradiation. A constant voltage step at the 10 V level is exhibited for the very low power levels of less than 1 mW.

10 V Josephson voltage standard circuit in CPS design with 17,000 SIS junctions. The microwave attenuation of the CPS with integrated Josephson junctions is about a third compared to the microstripline design. Therefore all 17,000 junctions can be arranged in only one CPS branch. At driving frequencies in the range of 70 to 75 GHz these voltage standard circuits generate stable quantised voltage steps at 10 V with a current-step-width of about 20 μA [2]. The CPS design will also be applied for programmable voltage standard circuits in SINIS technology.

At the IPHT the Josephson voltage standard circuits are tested in a measuring device which looks similar to the primary voltage standard at PTB. The test rack is shown in Fig. 3. At the top of the cryoprobe which is cooled in a helium dewar the filter box, a manual microwave attenuator and the Gunn oscillator with a directional coupler and an isolator can be seen. The frequency of the Gunn oscillator is stabilized to 10^{-10} by phase locking with a source locking counter. The extremely accurate 10 MHz output frequency of a GPS receiver serves as the external clock of the counter.

Other precision instruments such as pico-voltmeters and femto-ampere-meters will benefit from the advantages of the Digital SQUID discussed below. The market for such instruments is not large, but it will certainly grow in the near future.

There is also a demand for *high-speed detectors* with higher speed/higher resolution A/D and D/A converters in all kind of signal detectors, e g detectors in high-energy physics. Flash-type A/D converters are attractive by virtue of their simplicity (using n periodic comparators, as compared to their semiconductor counterpart, where 2^n comparators are required) as well as their speed advantage, and will find applications in digital *real-time processing* of signals. Their ability to directly digitize HF signals for measurements on microwave systems and equipment at very high frequencies and for very broad frequency bands, is a unique feature.

2.3.3. Digital SQUIDs

Digital SQUIDs essentially increase the linearity, the speed, and consequently the slew rate of the equivalent

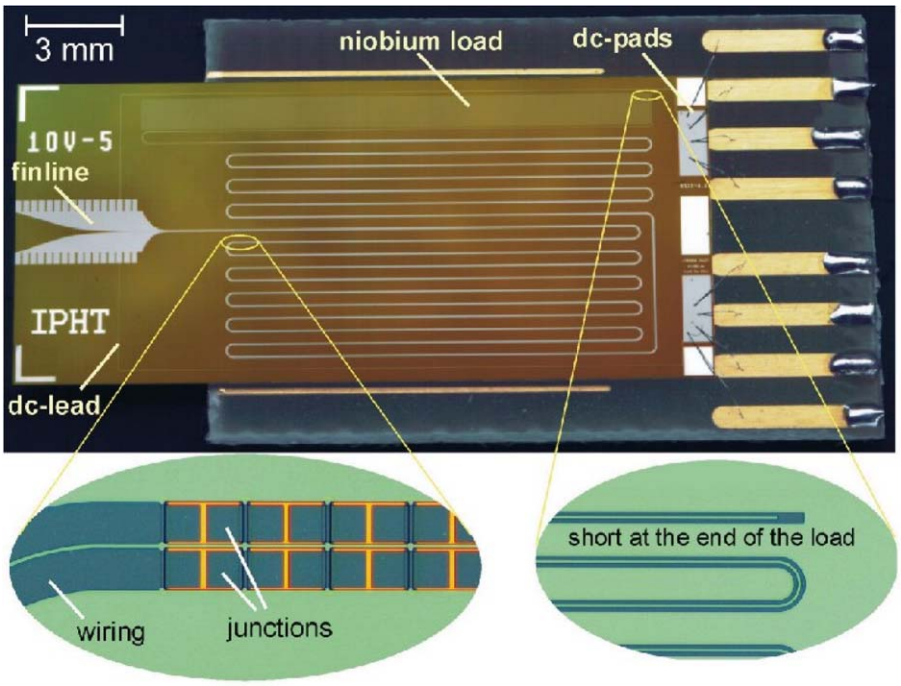


Fig. 2. Ten volts Josephson voltage standard circuit in CPS design with 17,000 SIS junctions. The junction size is 31 μm × 32 μm and the spacing between the two strips is 3 μm, see in the inset.

Fig. 3. Measuring device for the test of Josephson voltage standard circuits at the IPHT Jena. It looks similarly like the primary voltage standard at the PTB Braunschweig.

analog SQUIDs, in addition to suppressing the temperature drift of the sensor. Also, the sensitivity is somewhat improved because of the lower noise contribution of the read-out electronics. The advantages of the digital SQUID are therefore essential for portable and open environment sensor systems; for medical diagnostics and imaging, for non-destructive testing (NDE) of materials and for geophysical surveying. And digital SQUIDs will certainly relax constraints on system design for the other applications (e.g. MEG, where shielding is a significant part of the costs).

The digital interface with room-temperature electronics will also make digital SQUIDs attractive for gradiometry involving a large baseline or operating at some distance from the ground, in e.g. geophysical surveying or oil prospecting.

2.3.4. Ultra-fast packet switches

Ultra-fast packet switches in ultra-broad-band telecommunication networks, both terrestrial and satellite-based, are often said to be promising applications of the SDE technology, in spite of the fact that there are at present few real or perceived needs for such ultra-fast switches by the telecom industry, neither in copper nor opto-fiber networks. In the realm of optical fiber based communication, wavelength division multiplexing (WDM) and nonlinear multiplexing developments have practically closed the application window for SDE. The maximum modulation frequencies of laser diodes and modulators (of 10–40 GHz, i.e. relatively low with respect to SDE), make WDM a natural technology choice.

However, this pessimistic forecast for SDE could be completely reversed, if e.g. an RSFQ-pulse driven high-speed optical modulator, providing the hitherto missing direct coupling between the RSFQ and the photonic domain, was invented. (Such a device would also make the optical fiber an ideal interface between an RSFQ chip at 4 K and room-temperature electronics.) Future important niches for SDE could then develop e.g. in the form of high-speed add/drop multiplexers in very high-speed fiber networks.

2.3.5. PetaFLOP supercomputers

PetaFLOP supercomputers are a class of massively parallel processing computer architectures, in which RSFQ processors, an RSFQ-based crossbar switch core and Josephson transmission line (JTL) interconnects are essential enabling technology components. One million 1 GHz processors are needed to work in parallel, accessing each other and a large semiconductor memory bank (in the order of 30 terabytes) through a very fast central crossbar switch structure. The task of building a computer capable of 10^{15} floating-point operations per second (FLOPS) would be virtually impossible without LTS-RSFQ technology for, above all, power consumption reasons.

A "pre-study" of a PetaFLOP project was started in the early 1990s. The third phase (of in total five phases of the multi-billion US dollar project) was started in the year 2000. If the project gets funded to the expected level, it will have a profound influence on the field of LTS-based superconductor electronics, and speed up the long delayed development of a sub-micron Nb technology.

Even if the daunting goal of a PetaFLOP computer is not reached, an "intermediate result" in the form of TeraFLOP desktop PCs, could open up a multi-billion dollar market, given the expected development of the niobium and the cryo-cooler technology, as has been pointed out by Prof. K. Likharev at State University of New York at Stony Brook, and others.

2.4. LTS versus HTS technology

In the above account no reference has yet been made to the fact that there are two different kinds of SDE: one based on "low temperature superconductors" (LTS) and the other on "high temperature superconductors" (HTS). The LTS-SDE exists as a relatively mature Nb-based "large scale integrated" technology with a reasonable yield, and it can relatively easily be improved in terms of J_c ($>10\ \mathrm{kA/cm^2}$) and minimum feature size. The HTS-SDE, mainly based on the YBCO material, is still in its infancy.

HTS Josephson junctions promise about 10 times a higher circuit speed than LTS (due to the 10 times larger I_cR_n product of HTS) and have the additional advantage of being of the "self-shunted" type, eliminating the need for chip area-wasting external shunts. The present main problem with HTS-SDE is a more than twice too large a spread in the HTS Josephson junction parameters, which limits its use to circuits with low complexity (of 10–100 JJ's). In spite of these drawbacks HTS-SDE is expected to have important niche applications in hand-held equipment and satellite payloads, where low weight, size and cooling power consumption (as compared to those for LTS) is a decisive issue. In large-scale integrated RSFQ circuits, however, HTS faces fundamental as well as technological problems, as the advantage of operating at higher temperature is diminished by the increased thermal noise. The increased thermal noise can be counteracted by increasing the critical current of the junctions, but this, in turn, puts severe constraints on loop inductances and, consequently, on the circuit design. In spite of impressive improvements in HTS materials growth and Josephson junction technology in recent years, considerable progress is still required in order to reach an acceptable level of integration of, say, 10,000 junctions per RSFQ chip. Within the next 5–10 years it is therefore a safe prediction that all RSFQ circuits with a complexity exceeding 1000 junctions will use LTS, Nb-based technology. This is the more plausible considering the vast improvement potential of the Nb technology (from the current primitive 3.5 μm JJ technology with external shunts wasting chip area to a 0.4 μm technology with self-shunted JJs).

2.5. Cryo-cooler technology

A closed cycle cryogenic refrigerator (or "cryocooler") is an essential component of any superconductive electronic system. Hence, the availability of long operating lifetime, energy efficient and reasonably priced cryocoolers is universally considered an imperative for the commercial acceptance of SDE. The "cooling penalty" (that is, the overhead for cryogenically cooling electronic systems in terms of additional electrical power, mass, volume and cost of the cryocooler and the cryogenic enclosure) for a system operating at 4 K is very severe, while for higher operating temperatures, it is less severe as illustrated in the graph

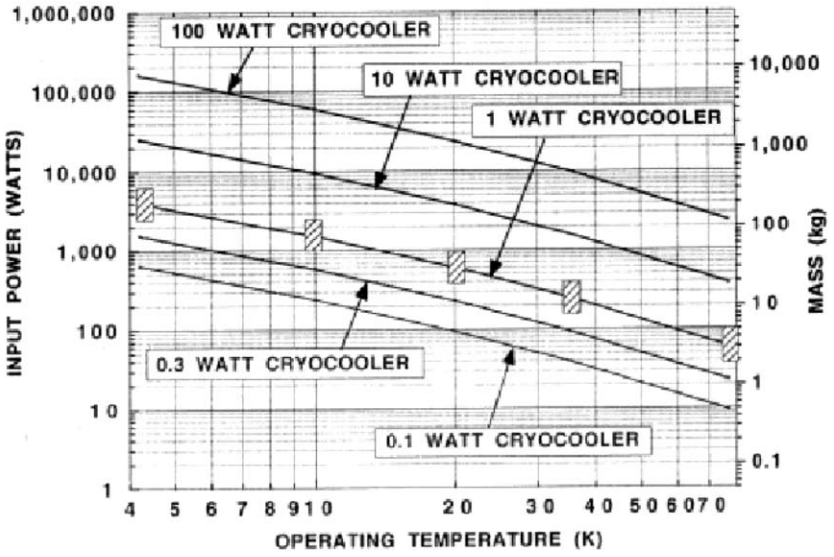


Fig. 4. Trend chart for power and mass versus operating temperature for cryogenic refrigerators with various values of cooling capacity. (Original by M. Nisenoff.)

of Fig. 4. (This graph was prepared by Martin Nisenoff, Washington, and is enclosed with his kind permission.)

The available cryogenic refrigeration systems are currently made for three diverse user communities. The military requires small (less than 1.75 W at 80 K) cryocoolers for cooling infrared detectors and imagers. These coolers, built to satisfy military specifications for dimensions, weight and functionality, require 4000-h MTBF (mean time between failures) and typically cost about 5000–10,000 Euros. About 100,000 such coolers have been built for both the military and commercial infrared surveillance communities.

The second class of cryocoolers, that have been built in quantity, are cryogenic vacuum pumps (“cryopumps”), which have been built to condense gases (other than helium) from thin film deposition systems. These cryopumps are not very energy efficient and are relatively massive but they have operating lifetimes of more than 5–8 years provided annual maintenance is done to the compressor. About 100,000 cryopumps have been sold at near 15,000 Euros.

The third class of cryogenic refrigerators are built in very limited quantities, and are cryocoolers for space applications where the heat loads are typically less than 1 W (although several larger units have been built) at operating temperatures from 100 K down to 10 K. The space coolers are energy efficient, compact, light weight and have operating lifetimes, without maintenance, of more than 5 years. BUT they cost from 500,000 to 1,000,000 Euros.

Cryocoolers made for these three diverse user communities do NOT satisfy the needs of SDE applications. For these applications the requirements for a cryocooler with a given cooling capacity (“lift”) at a specified operating temperature would be small size, good energy efficiency, long operating lifetime without maintenance AND with very modest cost (about 10,000 Euros, or less than 10% of the total superconductive system cost) when manufactured in medium quantities. The development of such coolers would require a large capital investment (in the order of 2–10 MEuros). The problem is that the SDE community is not yet able to make a strong case that the market WILL be large enough to warrant such a financial investment.

Table 2 contains “targeted” goals for SDE cryocoolers with 1 W heat lift and operating at respectively 4.5, 10 and 65 K. The input power figures assume that a Carnot Efficiency of near 10% can be achieved. Cryocoolers with

Table 2
“Targeted” goals for commercial cryocoolers suitable for SDE

Operational temp	4.5 K	10 K	25 K	65 K
Heat lift	1 W	1 W	1 W	1 W
Input power	1500 W	500 W	150 W	36 W
Mass	50 kg	20 kg	7 kg	2 kg
Volume	~0.2 m^3	~0.05 m^3	~0.01 m^3	~0.002 m^3
Cooldown time	30 min	30 min	30 min	30 min
Lifetime—without maint.	>40,000 h	>40,000 h	>40,000 h	>40,000 h
Cost				
if 100 units/yr	15–25 k€	10–15 k€	7.5 k€	5 k€
if 1000 units/yr	10 k€	7 k€	5 k€	3 k€

10% Carnot Efficiency have been realized for a number of space cryocoolers designed to operate in this temperature range and with heat loads near 1 W. These goals are deemed to be difficult but achievable if sufficient R&D funds are made available.

Note: It should be pointed out that Table 2 only gives cryocooler data "renormalized" to 1 W of heat lift. In reality a Nb chip is expected to dissipate considerably less power than a similar HTS chip, but to make a meaningful comparison a much more detailed study, which takes also into account radiation losses and heat losses from input/output leads and support structures, must be made.

3. Circuit simulation and design for superconductor digital electronics

The capability of simulating and designing superconducting circuits is a key prerequisite for the development of devices ready for practical applications. Due to the existence of two major material classes—low-T_c (LTS) and high-T_c (HTS) superconductors—with different specific levels of technological maturity, the approaches for design and simulation are specific as well.

3.1. Simulation/design for circuits of low complexity

The major aim of using high-T_c superconductors in digital electronics consists in prospective operation temperatures far above that which is given by liquid helium cooling.

As a natural consequence of elevated operation temperature, the intensity of thermal fluctuations will be increased as well. In order to maintain the same level of immunity against the noise caused by these fluctuations, the critical current, at which the Josephson junction leaves the zero-voltage state, has to be elevated as well. One major idea of RSFQ logic circuits is the connection of Josephson junctions via inductances where the product of the Josephson junctions' critical current and the inductances is constrained by an upper bound of approximately the value of the flux quantum, i.e. $\sim 2.07 \times 10^{-15}$ V s. This leads to the necessity of designing very small inductances which should be provided with a high accuracy. Usually this requires sophisticated numerical procedures. Especially the parameter extraction, i.e. the calculation of designed and parasitic inductances, requires 3D numerical field computation. Moreover, because of the intrinsic peculiarities, the inductance of HTS thin-film structures is much more sensitive to the material properties, especially to the magnetic field penetration depth. The latter, in turn, depends on technological parameters and should be known accurately as well. Thus the layout development for HTS RSFQ circuits is a repetitive process of layout design, parameter extraction, circuit simulation, and re-design until the specifications are met under the given design constraints. This cycle, starting from an initial design and leading towards a prototype to be fabricated, is shown in Fig. 5.

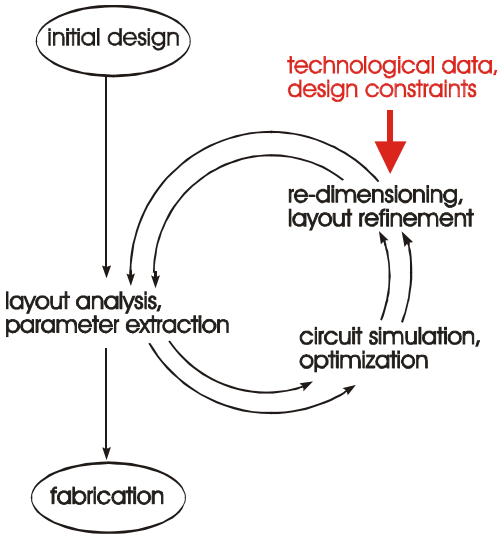


Fig. 5. Design flow for circuits of low complexity (small- to medium-scale superconducting digital circuits).

HTS RSFQ circuits are typically of low complexity. At this stage, it is appropriate to use small-scale analog circuit simulators which are specially designed for analyzing superconductive circuits as well as for studying circuit dynamics. For better efficiency, it will be necessary to achieve a convergence towards one common standard in order to exchange simulation models and intermediate results between the groups.

A similar situation holds for the use of layout programs where a common data representation (favourably GDS), at least in the import/export filters, is to be established. In general, only layout programs with the capability for Electrical Rule Checking (ERC) and Design Rule Checking (DRC) should be used. For all activities, a major focus should be on reusability and portability.

An important topic in circuit design concerns the design for manufacturability. By means of standard methods for design centering, the tolerances of the elements which constitute the electrical circuit, i.e. mainly the Josephson junctions' critical currents and the inductances, are increased. As result, a circuit configuration is found which allows for a fabrication with the highest-possible yield. This design phase is referred to as yield-driven circuit optimization and represents a major prerequisite for successful fabrication.

A common issue in digital circuits with low switching energies is the question of maintaining sufficient immunity against thermal and other fluctuations. This is also true for the RSFQ technique. In order to evaluate the circuit designs in terms of prospective noise-induced bit error rates, it is of importance to consider the effects of thermal fluctuations already in the digital circuit simulation. This option, being regularly used by most of the design groups, provides for a means for working towards high operation stability of the circuit under consideration.

Recently, a new understanding of the relationships in RSFQ circuits under the influence of thermal noise has

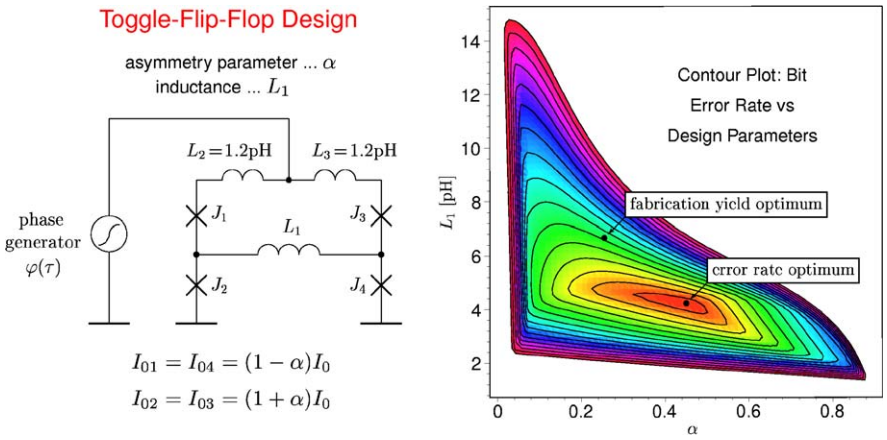


Fig. 6. Design and optimization of an HTS RSFQ toggle flipflop: bit-error rate versus design parameters.

been gained. Using a general mathematical model, it has been predicted that there are combinations of circuit parameters where the detrimental influence of thermal fluctuations is much less harmful than in common yield-driven designs. As an example, for an RSFQ toggle flipflop as shown in Fig. 6, the bit-error rate of the circuit can be significantly improved by adjusting the circuit parameters to the design values provided by the new method mentioned above [3].

The particular dependence of the bit-error rate on the most important circuit parameters is also shown in this figure. The controlled shift of the design parameters leads to six orders of magnitude improvement in the bit-error rate. An experimental verification of these new prospects for designs with better noise immunity is in preparation.

3.2. Simulation/design for integrated circuits

A different situation is given in the LTS technology where large-scale integrated circuits have already become feasible. Processes with defined parameters, narrow tolerances, and established design rules allow for integration levels at which simulation as well as circuit design and layout development on a component level are no longer efficient. Instead, single functional modules are developed and assembled within a cell library. The single cells are not too complex and can therefore be designed and optimized as outlined in Section 3.1. They are described in terms of structural, behavioural and geometrical data at different levels of abstraction and can be processed within contemporary design automation software. These systems support a hierarchical design style and are therefore capable of performing component-level, mixed-mode- and logic analysis. Tremendous performance gains in the simulation have been demonstrated this way. It has already been proven to be feasible to design complex digital circuits on a topological level using a top-down design methodology. Instead of starting with a schematic describing the electrical connections between gates, the design process begins with a description of the desired circuit behaviour. This

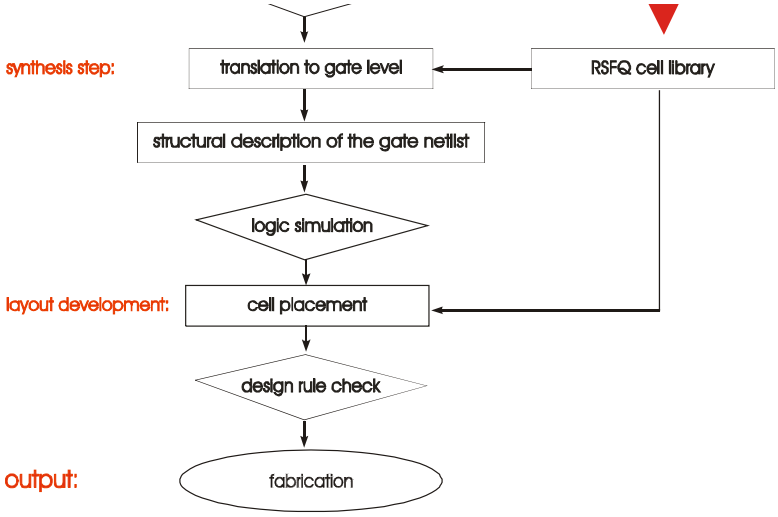


Fig. 7. Design process for highly complex integrated circuits originating from a behavioural specification.

contains the desired specifications and is given e.g. as VHDL which has a clear, standardized representation and is easy to assemble. Subsequently, the synthesis program generates a gate netlist according to the cells available in the library. The synthesis can be controlled by means of specifying constraints. Commonly, the synthesis result can be optimal with respect to maximum switching speed or smallest chip area. Fig. 7 gives an overview of a design process based on a behavioural description. This is an essential step towards designing circuits on customers' demand. The commercial software providing such features (e.g. CADENCE) can be afforded for reasonable costs under special circumstances for universities e.g. via EUROPRACTICE (http://www.europractice.com). Therefore, major emphasis should be put on exchangeability and reusability. As the time frame for establishing a technology-specific cell library of about 10 basic cells including yield optimization is about half a year for one person, it is of crucial importance to establish and maintain a stable technology for superconducting integrated circuits. This will include to designate a foundry. Because of the high costs, considerable expert knowledge and experience, and the demanding software maintenance it is reasonable to define dedicated sites to serve foundries. The actual software to be used is then to be defined, depending on costs and the software used at the foundry.

3.3. Common design infrastructure as implemented in the FLUXONICS circuit and cell library branch

Within the design branch of the FLUXONICS network (http://www.fluxonics.org), a significant level of establishing standards for the work of the European SDE community has been acquired. To maintain versatility of the RSFQ electronics, emphasis has been put on

- the development of the necessary set of basic circuits and gates needed in the synthesis of complex (integrated circuits),
- the development of efficient design tools and interfaces which are compatible with standard design software used in silicon microelectronics.

The network branch consists of a central design facility and dedicated design institutions in order to provide for design input to the foundries. Whereas the design sites develop cell libraries for low-, medium- and high-T_c SDE circuits, respectively, the central design facility takes care for consistency and correctness (DRC). Fig. 8 shows the network structure of the design branch.

The interaction including the information flow in the design network as well as the interaction with the foundries is shown in Fig. 9. Design data are transferred mainly as GDS files.

Currently, a considerable level of unification of the design tools has been reached [4]. The following tables provide an overview of basic tools for computer-aided design used by the FLUXONICS design groups. Table 3 gives an overview on the basic tools for computer-aided design used by the FLUXONICS design groups.

On this base, a high level of design reuse can be maintained. This will lead to a considerable acceleration of implementing system requirements in high-speed, low power superconductor electronics.

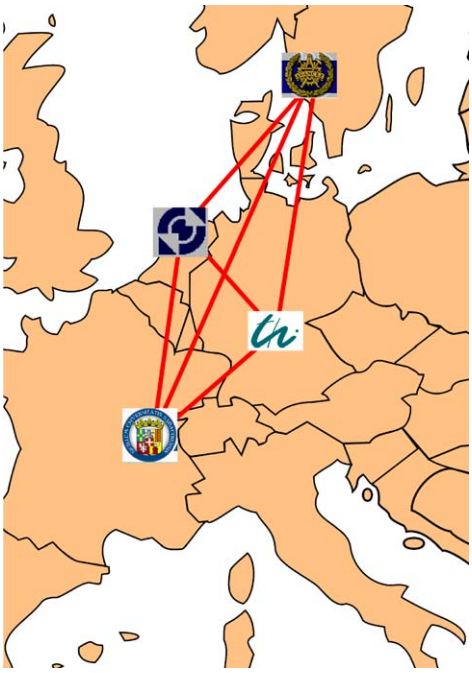


Fig. 8. FLUXONICS design institutions: Chalmers Technical University (Sweden), University of Twente (The Netherlands), Technische Universität Ilmenau (Germany), University of Savoie (France).

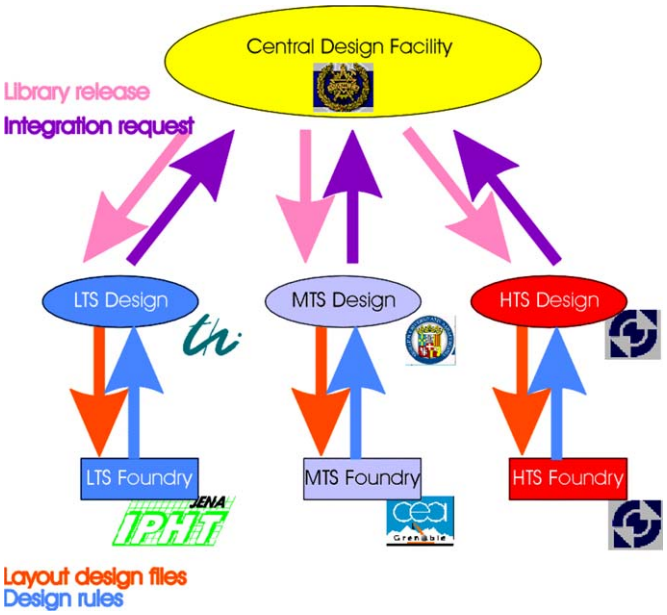


Fig. 9. Interaction of information flow in the design network as well as interaction with the foundries.

Table 3
Basic tools for computer-aided design used by the FLUXONICS design groups

Groups	Layout tool	Circuit simulator	Optimizer	Inductance estimator	Logic simulator
Chalmers University Gothenburg (Sweden)	Cadence	PSCAN	COWBOY	Lmeter & 3D-MLSI	Leapfrog VHDL
University of Twente (Netherlands)	CleWin	Jsim (with GUI)	WinS	Lmeter, Fast Henry	–
University of Ilmenau (Germany)	LASI Cadence	Eldo, Jsim, WinS	XOPT	Lmeter, MFB, SCIM	Eldo/Powerview
University of Savoie (France)	Wave-maker	Jsim (with GUI), WinS	WinS	Lmeter	–

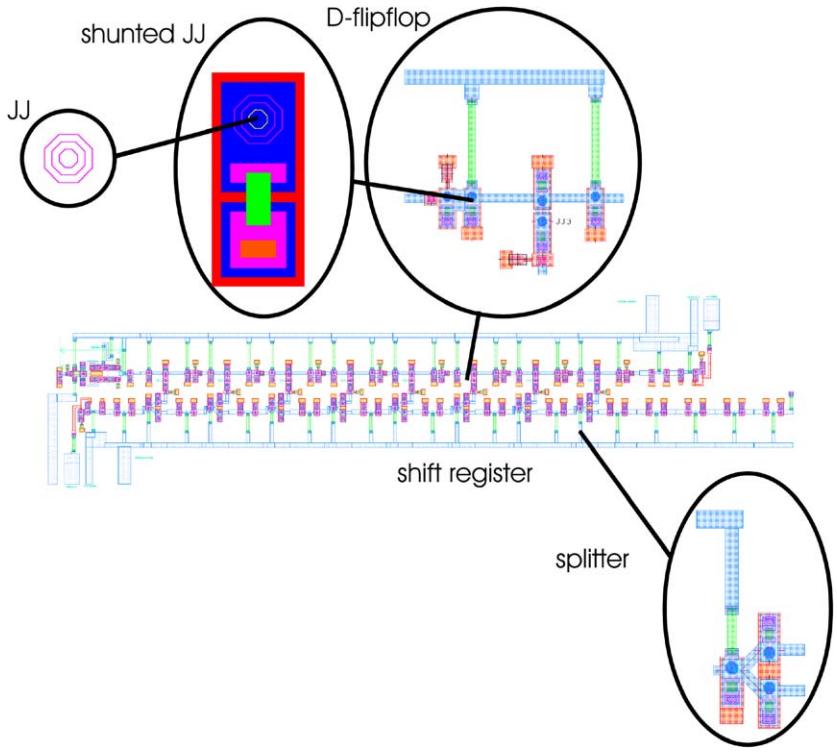


Fig. 10. Design of a superconductive RSFQ shift register together with other functional circuits for implementation in Nb/AlO_x/Nb technology.

As an example, Fig. 10 shows the RSFQ design of a superconductive shift register together with other functional circuits for implementation in Nb/AlO_x/Nb technology. The final design is entirely composed of sub-cells which are ordered hierarchically. Cell libraries of basic circuits were established in the framework of the FLUXONICS network. This was done in collaboration between TU Ilmenau and IPHT Jena as LTS foundry and between the University of Savoie and CEA Grenoble as MTS foundry.

3.4. Future goals

In order to develop viable RSFQ electronics on a system level, emphasis should be put also on

- the evaluation of alternative cell structures,
- the investigation of packaging designs for high-speed data transmission,
- the development of high-speed room-temperature interfaces.

This will form the necessary basis for a prospective rapid and systematic development of SDE designs.

4. Circuit fabrication

4.1. State of the art for superconducting circuit technology

4.1.1. LTS

Foundries for mainstream LTS technologies are established in the USA: Hypres and TRW for Nb/Al-oxide-technology based circuits and TRW for NbN-technology based circuits.

In Japan, NEC has a Nb/Al-oxide based foundry which only supplies circuits for the Japanese National Program.

The highest complexities achieved are an SFQ-RAM consisting of about 40,000 externally shunted Nb/Al-oxide junctions (NEC), a programmable voltage standard consisting of 30,000 SNS (Nb/PdAu/Nb) junctions (NIST), an array of 70,000 large-area SINIS junctions for a high-frequency programmable voltage standard (PTB), a micro FLUX processor consisting of 67,000 SIS junctions in

1.75 μm technology (TRW). A-to-D and D-to-A converters with a complexity of about 2000 junctions have been realized by Hypres, with performance that challenges the best semiconductor converters. The most "complex" circuits tend to be highly repetitive and fault tolerant. Junction standard deviations are not in general the limiting factor; it is occasional outliers that fall outside the normal distribution that limit circuit speed and complexity. In the following, two mainstream LTS technologies are described as they are available in Europe, Nb-technology and NbN-technology.

4.1.1.1. Nb-technology

- Description: complete wafer trilayer processes on the basis of SIS, SINIS and SNS sandwiches. S = Nb, I = Al-oxide, N = Al, PdAu, Cu, Ti, HfTi, or multilayer structures, e.g. HfTi/Nb/HfTi.
- Substrate: 3-in. Si-wafer, thermally oxidised.
- Complexity: up to 5 superconducting layers.
- Minimum linewidth: 3 μm.
- Failures: less than one junction per 1000 junctions.
- Operation frequency: up to 50 GHz.
- Tolerances (Table 4).
- Lithography: optical, proximity and projection.
- Operating temperature: 4.2 K.

Note: For low complexity circuits (20 junctions) a minimum junction size of $0.3 \times 0.3\ \mu m^2$ has been reached by e-beam lithography.

(1) *SINIS multilayer technology with internally shunted Josephson junctions*: To utilize the advantageous properties of internally shunted Josephson junctions implemented as the active circuit elements into superconductive circuit architectures, circuit fabrication at PTB is also focused on SINIS and SNS technologies [5]. In SINIS technolog, the fabrication process [6] is based on the standard process in PTB-μm SIS technology [7]. Fields of application are voltage standard circuits and RSFQ logic circuits [8].

Future development of LTS digital electronics based on RSFQ logic is strongly connected with an elevation of the integration level of circuits and, simultaneously, an increase of the operation frequency. SINIS technology based on conventional SIS production lines offers the possibility of satisfying most of these requirements. At PTB, for the fabrication of RSFQ circuits, a reliable technology process was developed in SINIS multilayer (Nb–Al/Al_xO_y/Al/Al_xO_y/Al–Nb) technology. The process was improved to raise the characteristic voltage of SINIS two-tunnel Josephson junctions up to $V_c = 245\ \mu V$ (corresponding critical current density: $J_c = 2.2\ kA/cm^2$). The area of the smallest junction is $A = 12\ \mu m^2$ [6]. In contrast to externally shunted Josephson junctions in SIS technology, the SINIS type junction offers the possibility of reducing the circuit area close to the size of the junction contact area.

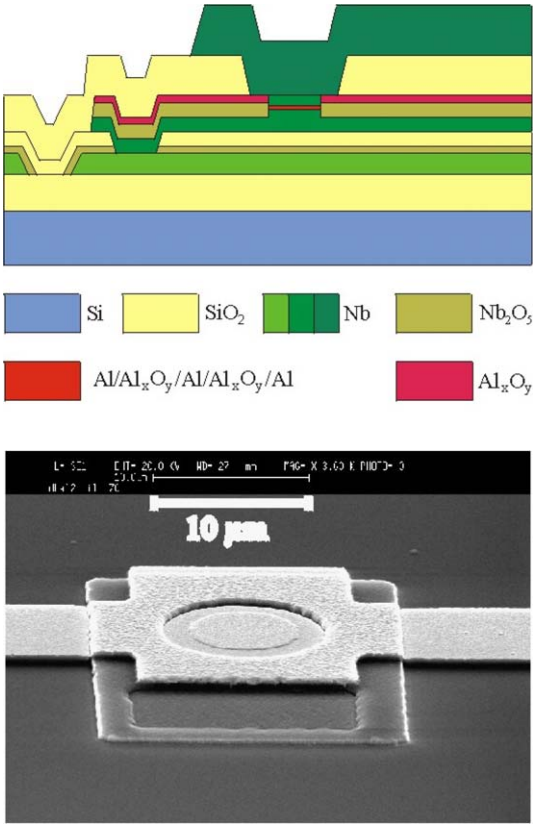


Fig. 11. Internally shunted Josephson junction in SINIS technology, upper: cross section (not to scale), lower: top view microphotograph (SEM).

Table 4
Tolerances for SFQ circuits on the basis of externally and internally shunted 3 μm linewidths Nb/Al-oxide technology (mainstream) for operation at 4.2 K

	Nominal value	Inter wafer tolerance (%)	On wafer tolerance (%)	On chip tolerance (%)
Josephson current density (SIS)	1 kA/cm^2	±30	±10	⩽±5
Josephson current density (SINIS)	1 kA/cm^2	±30	±10	⩽±5
Josephson current density (SNS)	100 kA/cm^2	±30	±10	⩽±5
Sheet resistance of Cr/Pt/Cr layer	1.0 ΩW	±7	±5	⩽±2
$L_□$: trilayer—groundplane	0.6 pH	±10	±5	⩽±2
$L_□$: wiring—trilayer (over groundplane)	0.7 pH	±10	±5	⩽±2
$L_□$: wiring—groundplane	0.9 pH	±10	±6	⩽±2
I_c	100 μA	±30	±10	⩽±5
I_cR_n	250 μV	±30	±10	⩽±5

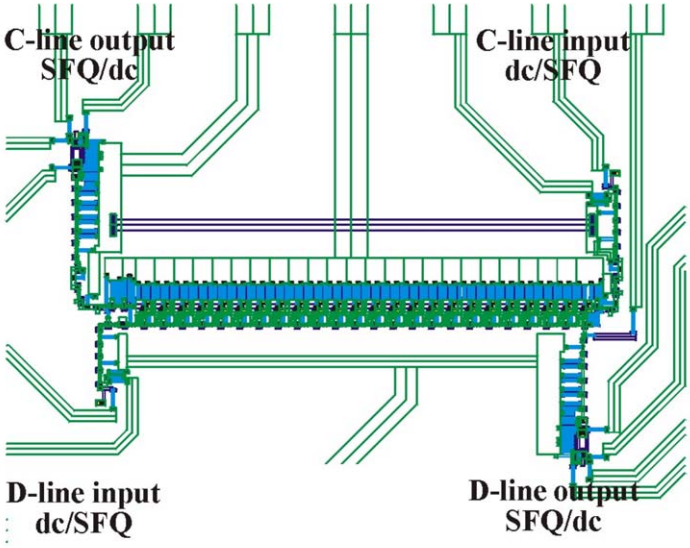
Table 5
SINIS technology parameters: sequence of layers of SINIS junctions

Function	Material	SINIS code	Thickness (nm)
Base electrode	Nb	S	170
Normal metal	Al		10
Tunnel barrier	Al_xO_y	I	1
Normal metal	Al	N	8–10
Tunnel barrier	Al_xO_y	I	1
Normal metal	Al		10
Counter electrode	Nb	S	100

Fig. 11 shows a schematic of the cross section of a SINIS junction and a top view microphotograph. The junctions realized show nearly hysteresis-free current–voltage characteristics (less than 15%), the intra-wafer parameter spread is smaller than ±10%. The main technology parameters are listed in Table 5.

SINIS Josephson junctions were successfully implemented in RSFQ circuits. At PTB, a large variety of RSFQ circuits of different designs were realized in SINIS technology and experimentally investigated, including dc/SFQ and SFQ/dc converters, Josephson transmission lines, T-flipflops, 3-bit pulse rate dividers, and shift registers. Correct function and high-frequency performance of RSFQ circuits were demonstrated. For T-flipflop circuits, the operational functionality was proved in the frequency range from dc up to nearly 200 GHz. The circuit parameters experimentally determined are about 750 A/cm^2 for J_c and about 170 μV for V_c. The bias current margins are larger than ±20% [9]. For digital circuit development and testing, shift registers serve as preferred devices as they incorporate all basic logic circuit components and are used as central modular parts in real-time digital processing applications. Fig. 12 shows RSFQ testing shift registers in SINIS technology.

The figure demonstrates single pulse operation of an 8-bit testing device at low clock rates. Bit pattern '1010000000000000' is applied to the data (D)-line input by the input current I_{D_in}. The shifted pattern is detected at the D-line output by the SFQ/dc converter, voltage V_{D_out}. The clock (C)-line is triggered by the input current



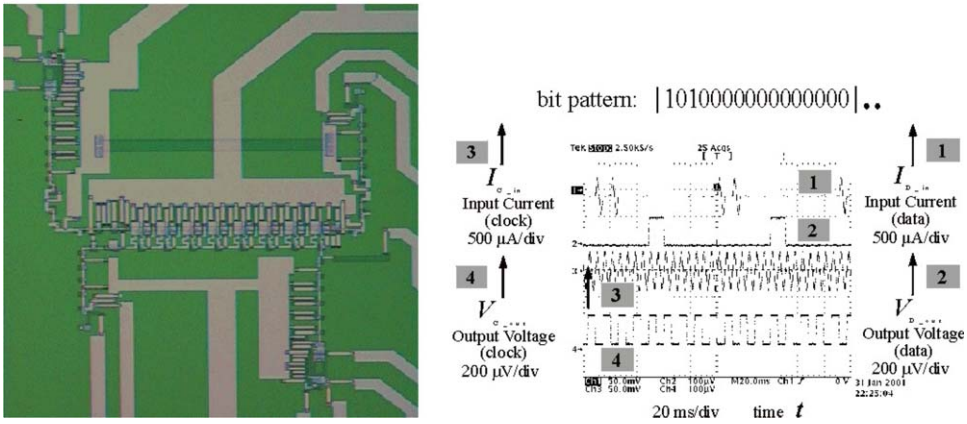


Fig. 12. RSFQ shift registers in SINIS technology, upper: layout of a 24-bit device, lower: 8-bit testing device, left: microphotograph (SEM), right: single pulse operation.

I_{C_in} with the continuous pulse sequence, '1111...1'. The C-line output is monitored by the voltage V_{C_out}. High frequency operation was tested in SFQ pulse train operation mode. Correct function was proved up to higher than 30 GHz for standard operation at constant preset circuit parameters.

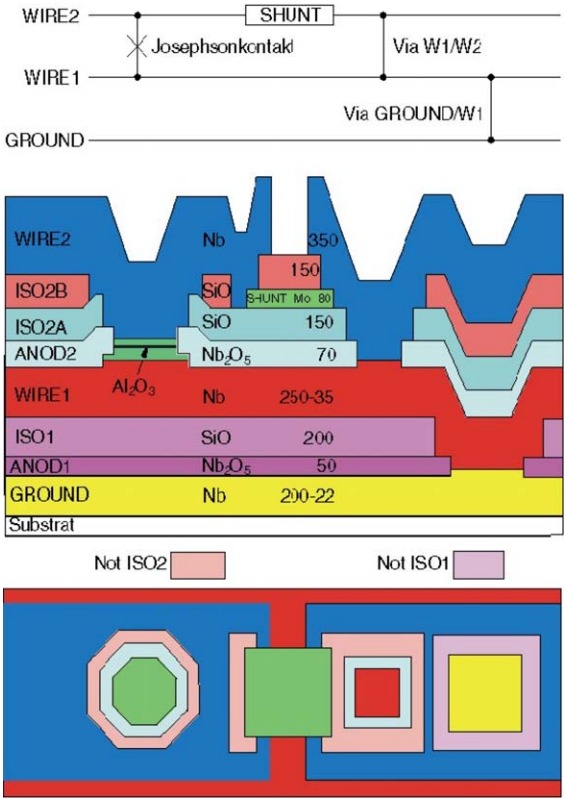


Fig. 13. Schematic, cross section and top view of a shunted and grounded Josephson junction for the IPHT Jena process. In the cross section the vertical scale is increased.

(2) *SIS trilayer technology with externally shunted Josephson junctions*: In SIS technology, for the IPHT Jena process, Fig. 13 shows a cross section and top view of a shunted Josephson junction on top of a superconducting ground plane. The complete preparation process comprises 12 photo mask steps listed in Table 6.

Thermally oxidized silicon wafers of 3-in. diameter are used as substrates. At first a Nb ground plane of a thickness of 200 nm is deposited by dc magnetron sputtering and patterned by reactive ion etching (RIE) in a CF_4 plasma. The isolation of the ground plane to the following parts of the circuit is made by the standard Nb anodization process up to a voltage of 25 V. This isolation is reinforced by an evaporated 200 nm thick SiO layer. In order to connect the ground plane to other metal layers, holes are opened by photo resist cover during anodization and by lift-off in the SiO isolation. The next fabrication step is the deposition of the base electrode consisting of 250 nm Nb by dc magnetron sputtering and its structuring by CF_4–RIE. The Nb/Al–Al_2O_3/Nb (60 nm/12 nm/30 nm) trilayer is deposited without vacuum interruption onto the Nb base electrode and patterned by lift-off. The areas of the Josephson junctions are defined by the following complete anodization of the trilayer counter electrode up to a voltage of 35 V. For the anodization all structures in the ground plane and in the base Nb electrode have to be connected to the anodization terminal. For the not grounded structures of the circuitry this is done with additional wires, which are removed by a cut etch step using RIE in a CF_4 plasma. A second SiO layer of a thickness of 150 nm is evaporated onto the sample to strengthen the anodic oxide. Contact holes in this SiO layer to the junction surface and to base Nb electrode are opened by lift-off.

As shown in Fig. 13, these contact holes are allowed to be larger than the Josephson junctions, because the isolation near the junctions is provided by the anodic oxide.

Table 6
Positive layout polarity means to design the physical structures as seen on the screen, negative means to design holes in the material

Mask	GDS II-No.	Name	Layout polarity	Color	Material	Thickness/nm	Description	Mask polarity
A	1	M0	Positive	Yellow	Nb	200	Ground plane	Dark
B	2	I0A	Negative	Magenta	Nb_2O_5	50	Holes in anodisation	Dark
C	3	I0B	Negative	Magenta	SiO	200	Holes in isolation	Clear
D	4	I0C			SiO		Reserved	
E	5	M1	Positive	Red	Nb	250	Wiring 1	Dark
F	6	T1	Positive	Cyan	Nb/Al/Nb	60/12/30	Trilayer package	Clear
G	7	I1A	Negative	Light blue	Nb_2O_5	70	Holes in anodisation, definition of junction	Dark
H	8	C	Positive	Light gray	–	–	Cutting of bridges for anodisation	Clear
I	9	I1B	Negative	Light blue	SiO	150	Holes in isolation	Clear
J	10	R1	Positive	Green	Mo	80	Resistance layer	Clear
K	11	I2	Negative	Coral	SiO	150	Holes in isolation	Clear
L	12	M2	Positive	Blue	Nb	350	Wiring 2	Dark
M	13	R2	Positive	Dark green			Bond pads, optional	Dark

Clear mask polarity means that the mask is transparent wherever the patterns are drawn and dark means the opposite case.

Next, as resistive layer, a Mo film of a thickness of 75 nm is sputtered and patterned by lift-off to form the resistors. A third 150 nm thick SiO layer is evaporated onto the sample to strengthen the isolation of different metal layers and to protect the Mo film against environmental influences. The circuits are completed by sputter deposition of a 12 nm Al etch stop and a 350 nm Nb wiring layer. The Nb is etched with a CF_4 RIE process. The Al etch stop layer prevents an over etch into the Mo resistive film and is removed by wet chemical etch after the Nb structuring process. For better bonding conditions the pads are optionally covered by Au. The described technological process was used for the fabrication of Josephson junctions with areas ranging from 10 μm^2 to 75 μm^2, junction arrays, resistors, arrays of connections between different metal layers and inductances. The current density of the trilayers was set to a nominal value of 1000 A/cm^2 and the sheet resistance of the Mo resistor layer to 1 Ω. The specific capacitances of the Josephson junctions have a value 4.5 μF/cm^2 and were determined from measured voltages of zero Fiske Steps of long junctions. Tables 7 and 8 show typical parameter spreads of Josephson junctions and stripline inductances. In Table 9 typical values of area, critical current, diameter, and shunt resistor for Josephson junctions are noted.

Fig. 14 shows a RSFQ circuit produced with the described IPHT Jena process. This traditional type of RSFQ process is well established and forms a stable base for the further process development to circuits of a higher level of integration.

This process will be further qualified by the replacement of the SiO isolation films by CVD-SiO_2 films for better edge coverage. Intrinsically shunted junctions like SINIS (see Section 4.1.1) and SNS junctions offer the advantage of higher packaging densities and decreased parasitic inductances, for application voltage standard circuits [10], and in RSFQ circuits [11]. But SNS junction areas have to be in the deep submicron range for appropriate critical currents. To realize this decrease of the minimum junction size the transition from proximity lithography to DUV projection lithography or direct e-beam exposure is necessary and the junction isolation has to be done by a kind of damascene technique with SiO_2 instead of the current anodization process. This process has to be development in the next future. Series arrays of 2000 Nb–Ti–Nb SNS junctions with junction areas of $0.6 \times 0.6\ \mu m^2$ have been realized at the IPHT and successfully tested in a voltage standard circuit designs.

4.1.1.2. NbN-technology

- Description: complete wafer trilayer processes on the basis of two sandwich versions: SIS (for 10 K) and S^*SIS^* (for 7 K). S = NbN, S^* = Nb, I = MgO.

Table 7
Spread of Josephson junctions parameters

	Nominal value	Intra wafer tolerance (%)	On wafer homogeneity (%)	On chip homogeneity (%)
Josephson current density	1000 A/cm^2	±20	±15	⩽±5
Sheet resistance of Mo-layer	1.0 Ω	±20	±10	⩽±5

Table 8
Spread of stripline inductance

Layer	$L_\square$	Intra wafer tolerance (%)	On wafer homogeneity (%)	On chip homogeneity (%)
M1–M0	0.52 pH	±10	±5	⩽±2
M2–M1 (across M0)	0.64 pH	±10	±5	⩽±2
M2–M0	0.81 pH	±10	±6	⩽±2

Table 9
Typical values of area, critical current, diameter, and shunt resistor for Josephson junctions

A/μm^2	12.5	17.7	20.6	23.8	30.8	36.7	59.9
I_c/units[a]	1.00	1.50	1.75	2.00	2.50	3.00	5.00
I_c/μA	125	187.50	218.75	250	312.50	175	625.00
∅/μm	3.9	4.6	5.0	5.4	6.1	6.7	8.5
C_J/pF	0.625	0.885	1.03	1.19	1.54	1.835	3.0
R_s/Ω[b]	2.10	1.40	1.20	1.05	.85	.70	.40

[a] The normalized I_c values are for developers using PSCAN. The unit I_c is 125 μA.
[b] The R_s value is calculated for adjusting $\beta_c = 1$.

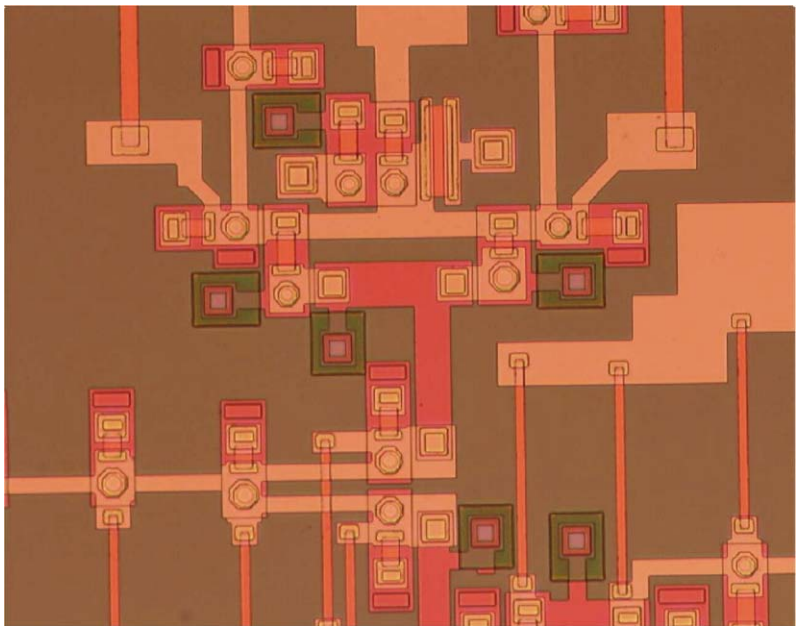


Fig. 14. Nb/Al_2O_3–Al/Nb circuit produced with the IPHT Jena process.

- Feasibility of SINS, SNS and SINIS where N: Ti(N), Ta(N) or Nb(N).
- Substrate: 3-in. Si-wafer, R-Sapphire and SOI (Silicon on Insulator) buffered with MgO.
- Complexity: up to 2 epitaxial layers on R-Sapphire and up to 5 superconducting layers on micromachined SOI.
- Minimum linewidth: 3 μm.
- Failures: less than one failure per 1000 junctions.
- Operating frequency: up to 200 GHz.
- Tolerances (Table 10).
- Lithography: UV optical contact/Si-MOS facility deep UV steppers.
- Operating temperature:
  up to 10 K for all NbN (SIS self shunted version).
  up to 7 K for the hybrid electrode (S^*–SIS–S^*) Nb/NbN version.

Note: For low complexity NbN circuits, deep submicron junction size has been fabricated by e-beam lithography and by other techniques (AFM lithography,...), but the choice is a deep UV planarized nitride technology also presently developed on 8-in. Si wafer under a CEA-Leti-Plato project.

- Comparison of technologies (Table 11).

Table 10
Tolerances for SFQ circuits on the basis of externally (4 K) and internally (10 K) shunted 3 μm linewidths NbN/MgO/NbN technology (mainstream) for operation at 4 K or 10 K

	Nominal value	Inter wafer tolerance (%)	On wafer tolerance (%)	On chip tolerance (%)
Josephson current density				
(a) 4 K (S^*–SIS–S^*)	1 kA/cm^2	±25	±10	⩽±5
(b) (SIS—10 K self-shunted)	10 kA/cm^2	±30	±15	⩽±5
Low sheet resistance (Mo)	0.8 ΩW/□	±10	±5	⩽±5
High sheet resistance (NbN_x or TaN_y)	10 ΩW/□	±10	±5	⩽±5
$L_□$: wiring—groundplane	1.5 pH/□	±10	±6	⩽±3
I_c	0.25 mA	±30	±15	⩽±5
I_cR_n				
(a) 4 K	0.5 mV (for $J_c = 1$ kA/cm^2)	±30	±15	⩽±5
(b) 10 K	1 mV ($J_c = 10$ kA/cm^2)			

Table 11
Comparison of advantages and drawback of NbN technology versus Nb technology

Advantages of NbN technology versus Nb technology	Drawback of present NbN technology versus Nb technology
Higher operating temperature. More efficient cooling	Larger inductance $L_□$ values with lower reproducibility and T stability
Higher cut-off frequency, higher output voltage. Efficient optoelectronic and semiconductor interfaces with NbN ($I_cR_n \sim 2$ mV for shunted junctions)	Less mature *but* higher compatibility with semiconductor processing
Lower thermally activated bit error rate at 4.2 K in RSFQ cells	More sensitive to flux trapping (lower H_{c1}) *but* better flux pinning

High current density SIS–NbN/MgO/NbN (1 μm diameter) junctions with JC in the range of 10–20 kA/cm^2 have been routinely obtained on 3-in. wafers at CEA-Grenoble but also in few other places in the world for developing 1 THz range SIS mixers for radioastronomy. By choosing proper heat treatments and processing steps, it is possible to achieve large energy gap $2\Delta_0 = 6.2$ meV and large I_cR_n products for such junctions with tuned RC cut-off close to 1.4 THz. Such a NbN SIS technology has been oriented for making RSFQ junctions with minor modifications in the processing: self-shunted junctions with I_cR_n products as large as 2 mV at 4 K for J_c of the order 40 kA/cm^2 and I_cR_n products as large as 1 mV at 10 K for J_c of the order 15 kA/cm^2 are now achieved. The target to achieve such high I_cR_n products, self-shunted junctions with J_c in the order of 5–10 kA/cm^2 is approached in few places by using barrier materials choice including MgO, AlN, Ta(N), Ti(N), Nb(N),... The present NbN technology opening the possibility of circuit operating temperature around 10 K appears very reliable due to the high mechanical and chemical stability of cubic B1 nitride phase.

RSFQ circuits with few hundred junctions are now accessible to the present 3 μm linewidth NbN CEA-Grenoble technology, while the planarization of 0.4 μm diameter junction by using the CEA-G Leti-Plato technological plateform (for 8-in. Si wafers) opens the medium term possibility to achieve RSFQ circuits with more than 100 k junctions per chip.

Fig. 15 shows a 8 BIT shift register circuit from the first FLUXONICS mask-set processed with a 3 μm linewidth technology developed at CEA-Grenoble by the MTS Foundry. NbN/MgO/NbN-1 kA/cm^2 critical current density junctions are combined with Nb groundplane and Nb wiring lines leading to reduced square inductance values. The design of this MTS shift register circuit has been done at University of Savoie as shown on Fig. 9.

4.1.2. HTS

Digital circuit fabrication in HTS is much less mature than LTS technology. High critical current junctions and tight control of stray inductance are vital for HTS, while in LTS they are merely desirable. On the other hand, LTS circuits must comprise more functionality than HTS to compensate for the increased cooling burden.

A number of companies have a trilayer technology based on ramp-type technology. In the USA, Conductus, Northrop-Grumman and TRW have been developing HTS circuit technologies with major government funding, but this program has come to an end. However some companies continue their activities on a moderate scale using their own funding. There is no University activity in HTS logic technology in the USA. In Japan, two major programs on digital superconducting logic are running (HTS and LTS), with participation by NEC, Toshiba, Hitachi and University groups. The best I_c parameter spread reported for junctions on a groundplane is 15% (100 junctions @ 4 K) using artificially engineered interfaces as barrier. Without groundplane the spread is typically lower, i.e. 10%. Remarkably enough the spread of these junctions

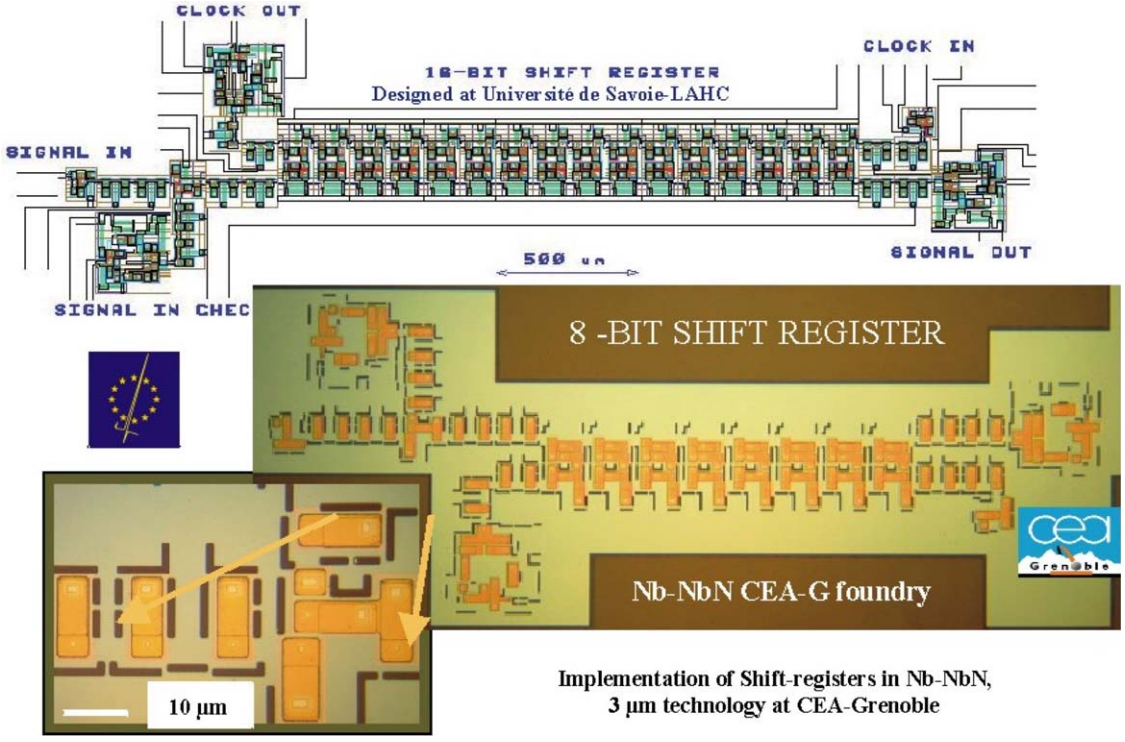


Fig. 15. Implementation of a 8 bit shift register circuit with a new Nb–NbN 3 μm technology developed at CEA-Grenoble MTS-Foundry; (the design of a similar 16-bit shift register done by University of Savoie is represented in the upper part of the figure).

increases with operating temperature. It also increases with decreasing current density.

In Europe, multilayer digital circuit technologies are being developed at Chalmers, DERA, Jülich, Thomson and Twente. Other laboratories (NKT, Hamburg, Jena) have multilayer SQUID technologies, which might in principle extend to digital logic. Presently work at DERA has shifted its focus to SQUID technology.

Most of the laboratories actively involved in HTS logic have demonstrated circuits up to a complexity of 10–20 junctions. Only one of these, a sampler (NEC), performs a complete function and could be a commercial product. As yet, there is no consensus on the preferred junction technology, although it is widely accepted that a multilayer circuit technology is essential. It seems likely that the preferred operating temperature will be determined, at least in the medium term, by the maximum permissible bit error rate in specific, economically viable, applications. The challenge of HTS SFQ is to identify these applications and develop a technology that can deliver them.

At present, there are three junction technologies being developed for logic circuits. These are two sorts of edge junctions (PBCO barrier and "natural" barrier) and junctions induced by damage. In none of these cases is the junction reproducibility very well established by published systematic statistics. This is simply a consequence of the scale of the effort deployed; all the groups must design and demonstrate functioning circuits and carry out technology research in parallel with benchmarking the technology.

With the limited evidence available, standard deviations of I_c around 10–15% are possible for all the above technologies. At least a factor of 2 improvement is needed for medium complexity circuits to give economic yields. The junction reproducibility required is directly linked to the minimization of stray inductance. Beyond this, further improvements in reproducibility could be translated into higher complexity or higher operating temperature.

A summary of the process developed at the University of Twente is given in Fig. 16 for the deposition and patterning steps in the total fabrication process of the ramp edge junction on top of the buried ground plane, and of the process developed at Chalmers University of Technology in Fig. 17.

As an example of a circuit that was fabricated and successfully tested at the University of Twente we present below the schematic diagram of a Σ–Δ modulator in Fig. 18 and a SEM micrograph of its actual layout in Fig. 19. Maximum operating speed was as high as 175 GHz at an operating temperature of 10 K.

At present the mainstream of the development is probably best characterized by:

Ramp-type technology:

- Description: all-epitaxial multilayer technology, YBCO/PBCO and interface engineered barriers.
- Substrate: $SrTiO_3$, buffered MgO and $LaAlO_3$.
- Complexity: up to 3 superconducting layers.
- Minimum linewidth: 3 μm.

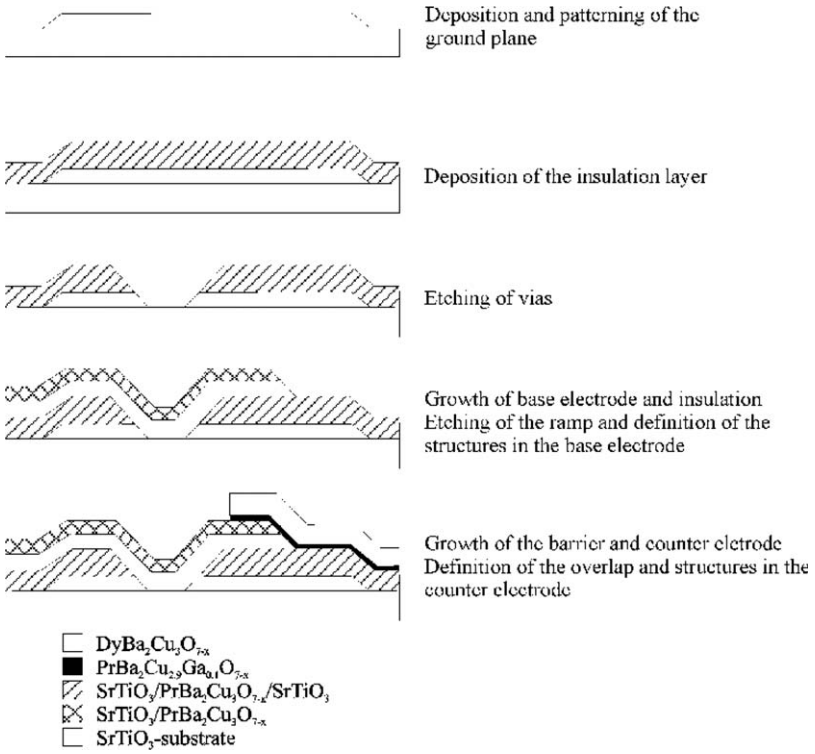


Fig. 16. Technology process developed at the University of Twente: overview of the ramp edge junction fabrication process with a buried ground plane.

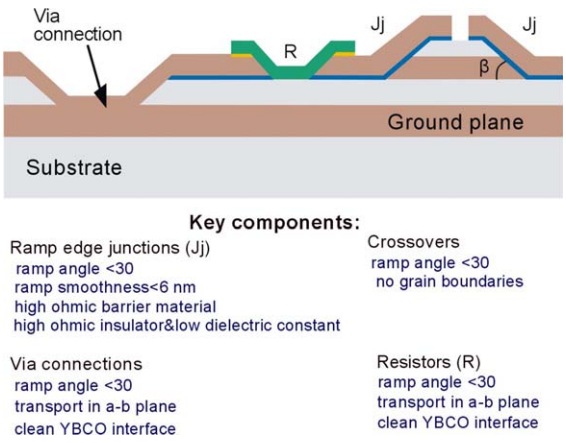


Fig. 17. Technology process developed at Chalmers University of Technology: integrated technology based on ramp Josephson junctions and a superconducting ground plane. (All ramps in the circuit: ramps for Josephson junctions, via connections and crossovers, are formed under substrate rotation during the ion milling. This allows for positioning all circuit elements by will at any place on the chip. All superconducting films and insulators are grown by pulsed laser deposition.)

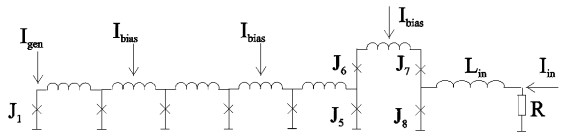


Fig. 18. Equivalent diagram of the Σ–Δ converter.

- Failures: Not a limiting factor.
- Operating frequency: up to 100 GHz at 40 K and 1 THz at 4.2 K.
- Tolerances (Table 12).
- Lithography: optical, proximity and projection.
- Operating temperature: 4.2–80 K (strongly dependent on application).

Note: HTS junctions are naturally shunted and resistors are only required for some specialised circuits.

4.2. Future developments (5–10 years)

4.2.1. LTS and MTS

The thrust of LTS technology development will be increased critical current density and finer linewidths, leading to increased circuit speed. To yield complex circuits, the number of junction failures must be reduced. Wafer size will increase to reduce manufacturing cost.

For standards and complex digital circuit applications, the technology is expected to be LTS (Nb or NbN) technology as follows:

- Description: complete wafer trilayer processes on the basis of SIS, SINIS and SNS sandwiches. S: Nb and NbN, I: Al-oxide (and MgO or AlN for NbN STJ), N: Al, or PdAu, Cu, Ti, HfTi, or multilayer structures, e.g. HfTi/Nb/HfTi, (NbN_x, TiN_y, TaN_z, for NbN JJs), ...

SNS technology offers a high potential to increase circuit integration. At PTB, a technology process for the fabrication of sub-micron SNS ramp-type Josephson junctions was developed, which allows these junctions to be used as

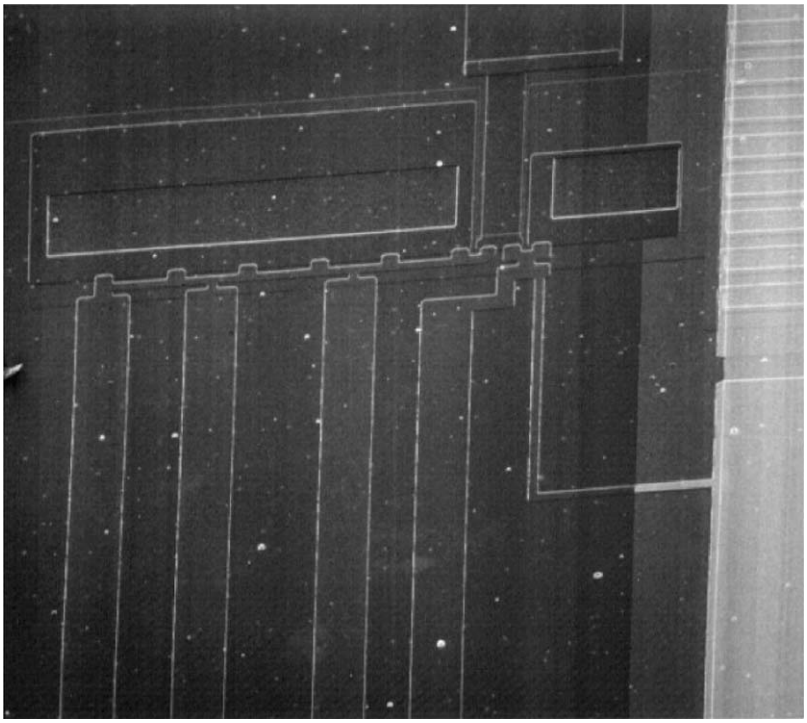


Fig. 19. SEM picture of the Σ–Δ modulator. The small dots on the surface are droplets from the pulsed laser deposition of the gold layer.

Table 12
Tolerances for SFQ circuits

	Nominal value	Inter-wafer tolerance (%)	On-chip tolerance (%)
Josephson current density	10 kA/cm^2	±20–30	⩽±10–20[a]
$L_\square$: trilayer—groundplane	~1 pH		⩽±10–20
I_c	0.5 mA		⩽±10–20
I_cR_n	0.5 mV (40 K)		
	6 mV (4.2 K)		

[a] Tolerance for closely spaced junctions: ⩽±5–10.

active elements in highly integrated circuits. Test circuits of large series arrays with contact areas below 0.4 μm^2 were realized, see Fig. 20. A high grade of reliability in circuit operation was proved for the implementation of Nb/HfTi/Nb ramp junctions in series arrays containing 10,000 SNS junctions (single contact area $A < 0.4\ \mu m^2$, N-layer thickness $d = 40$ nm, $V_c = 2.4\ \mu V$, $J_c = 10$ kA/cm^2). Under 1.5 GHz radiation, it was demonstrated that each single junction contributed to the expected constant voltage steps [8]. A considerable raise of the characteristic voltage was demonstrated for SN′S (Nb/HfTi–Nb–HfTi/Nb) multilayer structures (thicknesses of the inner N'-multilayer: HfTi (5 nm), Nb (10 nm), HfTi (5 nm)). For single junctions with contact areas of $A = 0.2\ \mu m^2$, characteristic voltages of $V_c = 460\ \mu V$ were achieved, together with critical current densities of $J_c = 210$ kA/cm^2 [11]. At further reductions in contact area, single SNS ramp junctions were realized down to 0.03 μm^2.

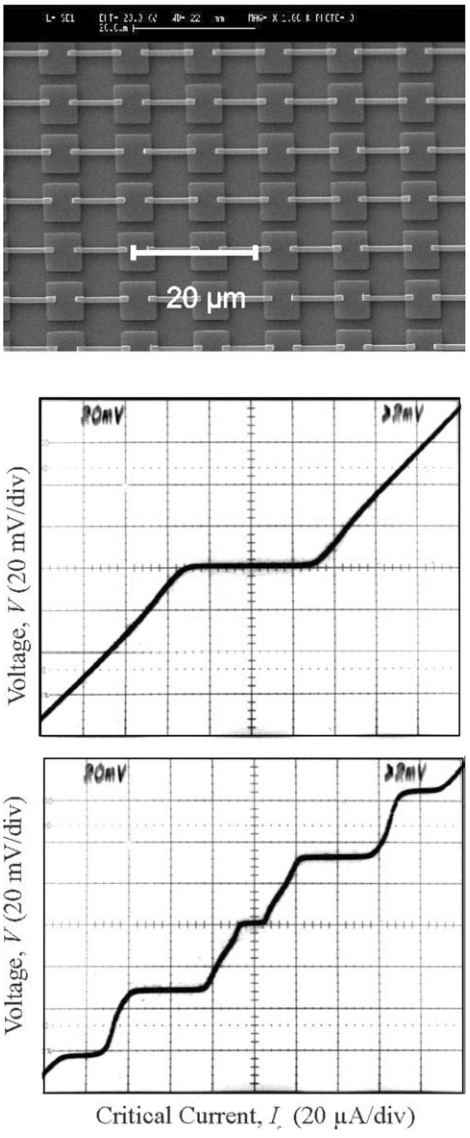


Fig. 20. Josephson series arrays containing 10,000 SNS Josephson junctions in ramp-type configuration, upper: microphotograph (SEM) (contact areas: $0.25 \times 1.3\ \mu m^2$, thickness of the N-layer: $d = 40$ nm), central and bottom: current–voltage characteristics of a 10,000 Nb/HfTi/Nb ramp junctions array, central: without microwave irradiation, bottom: under 1.5 GHz microwave irradiation.

Table 13 gives an overview on the prospective development of Nb circuits.

- Planarisation will be needed.
- Junction number: 200,000.
- Substrate: 4–6-in. Si-wafer, thermally oxidised *or SOI* (*same size*).
- Complexity: up to 5 superconducting layers.
- Minimum linewidth: 0.5 μm.
- Failures: less than one junction per 20,000 junctions.
- Operating frequency: up to 500 GHz.
- On-chip tolerances (junctions, inductances, resistors and connections) for SFQ circuits on the basis of externally shunted 0.5 μm linewidths Nb or NbN technology (mainstream): smaller than 5% all.
- Lithography: optical, projection, *Deep-UV Stepper*.
- Operation temperature: 4.2–10 K.

4.2.2. HTS

The main obstacle to overcome in HTS is the development of a technology with sufficiently high junction reproducibility and low stray inductances. This comprises:

- Tighter process control and improved choice of materials will push down parameter spread to about 5%. If we assume the present on-chip spread to be 15% we expect to be able to push this down to 10% in a few years time, whereas 5% may take 10 years to achieve. Here we use typical spread, not best result.

Table 13
Prospective development of Nb circuits

	Time				
	3 years				
Circuit type	10 V SIS standard with integrated SINIS-RSFQ circuit	10 V SINIS DC standard with integrated SINIS RSFQ circuit	SINIS RSFQ circuits: e.g. voltage multipliers a/d converters	1 V SINIS Arrays with binary subdivisions for 1 MHz DC switching	SNS Arrays with microwave circuits and SNS RSFQ circuits
Complexity	14,000 SIS junctions, +200 SINIS junctions	70,000 SINIS junctions + 200 SINIS junctions	200 SINIS junctions	8200 SINIS junctions	Up to 40,000 junctions in arrays and up to 1000 junctions in RSFQ circuits
Linewidth	5 μm	5 μm	2 μm	5 μm	1 μm
Electr. parameters	J_c(SIS) ≈ 150 A/cm^2, J_c(SINIS) ≈ 1 kA/cm^2	J_c(SINIS) ≈ 400 A/cm^2	J_c(SINIS) ≈ 3 kA/cm^2	J_c(SINIS) ≈ 200 A/cm^2	J_c(SNS) ≈ 10^5 A/cm^2
	I_cR_n ≈ 150 μV	I_cR_n ≈ 150 μV	I_cR_n ≈ 250 μV	I_cR_n ≈ 150 μV	I_cR_n ≈ 400 μV
Spread	5%	5%	5%	5%	5%
	Commercialised; transfer to foundry	Commercialised; transfer to foundry			
	6 years				
Circuit type		10 V SINIS arrays with binary subdivisions for 1 MHz DC switching with integrated SINIS RSFQ circuit	SINIS RSFQ circuits e.g. voltage multipliers a/d converters	10 V SINIS Arrays with binary subdivisions for 1 MHz DC switching with integrated RSFQ circuit	SNS Arrays with microwave circuits and SNS RSFQ circuits
Complexity		70,000 SINIS junctions + 200 SINIS junctions	2000 SINIS junctions	70,000 SINIS junctions + 200 SINIS junctions	Up to 100,000 junctions in arrays and up to 5000 junctions in RSFQ circuits
Linewidth		2 μm	1.5 μm	2 μm	0.5 μm
Electr. parameters		J_c(SINIS) ≈ 1 kA/cm^2	J_c(SINIS) ≈ 5 kA/cm^2	J_c(SINIS) ≈ 1 kA/cm^2	J_c(SNS) ≈ 10^5 A/cm^2
		I_cR_n ≈ 150 μV	I_cR_n ≈ 300 μV	I_cR_n ≈ 150 μV	I_cR_n ≈ 1 mV
Spread		3%	5%	3%	5%
		Commercialised; transfer to foundry		Commercialised; transfer to foundry	
	10 years				
Circuit type			SINIS RSFQ circuits e.g. voltage multipliers a/d converters		SNS Arrays with microwave circuits and SNS RSFQ circuits
Complexity			100 blocks a′2000 SINIS junctions or 20,000 junctions		Up to 200,000 junctions in arrays and up to 20,000 junctions in RSFQ circuits
Linewidth			1 μm		<0.5 μm
Electr. parameters			J_c(SINIS) ≈ 10 kA/cm^2		J_c(SNS) ≈ 1 MA/cm^2
			I_cR_n ≈ 300 μV		I_cR_n ≈ 1.5 mV
Spread			3%		5%

- More superconducting layers will reduce stray inductances. Here we do not mean just a ground plane, but an extra layer to further reduce stray. In LTS such a layer would not be needed for this purpose due to the lower London penetration depth of LTS. Furthermore also ramp-type technology gives rise to extra stray from the counter electrode. A top layer will also reduce this extra stray.
- Within 5 years circuit complexities of the order of 100 junctions may be achieved, and within 10 years this may increase an order of magnitude. Whether this will happen depends on the availability of resources to do the work.

The above is based on experience with ramp-type junction, whether the barrier consists of a deposited layer or an engineered layer. It is worth mentioning at this stage that also other technologies exist. Sometimes, as holds for bicrystal grain boundary junctions, junction parameter spread is not a big issue and product development is well underway. An example are SQUIDs for magnetometers and gradiometers. For some applications also BSCCO stacks may be useful. Examples are, detection/generation of electromagnetic radiation, the volt standard etc. Furthermore it would be highly advisable to put more effort in developing an all-thin film planar junction technology

as this facilitates circuit layout and minimizes stray inductances.

5. Interfacing and testing of RSFQ circuits

5.1. Status

The basic requirements are high test reliability and low test costs. The ability to test for failure operations is essential because of the high internal clock frequency. Built-In-Self-Test (BIST) and Design-For-Test (DFT) are appropriate solutions for high-speed on-chip testing using low-cost and low-speed testers.

Superconducting digital circuits of the Rapid Single Flux Quantum (RSFQ) family with Josephson current densities around 2 kA/cm^2 may be operated at 4.2 K with clock frequencies up to 50 GHz (1/3 of the plasma frequency). To operate these superconducting subsystems with semiconductor electronics mostly at room temperature properly designed input and output interfaces are needed. The interfaces must have an extremely broad frequency band in the order of 20 GHz for transmission and processing of picosecond pulses, a sufficiently large signal to thermal noise ratio and a bit error rate at least smaller than the subsystem to be tested. Moreover, the interfaces must take into account the relative large cross sectional dimensions of chip-to-chip interconnections compared to the miniaturized structures on the chip, different impedance, temperature, and voltage levels.

Before using superconducting subsystems, industrial customers want a pseudo-random bit sequence (PRBS) error test with the standard semiconductor equipment at room temperature, e.g. from Anritsu or Agilent where the number of errors between input and output patterns are counted bitwise. These PRBS pattern generators and detectors may work with large bit sequence lengths of $2^{31} \approx 10^{10}$ and in the Non-return-to-Zero-mode, i.e. the signal does not return to zero between consecutive ones.

Bitwise testing at very high speed up to 18 Gb/s has already been demonstrated with 1024 bit acquisition shift registers at input and output integrated on the same chip as the device to be tested. The output shift register can be read out at sufficiently low speed (30 Mb/s) and hence low error rate. Unfortunately, using the currently available Nb technology, devices or subsystems to be tested are not easily integrated on the same chip with acquisition shift registers of sufficient length (10^6 bit). 64 bit buffer shift registers have been tested up to 8 Gb/s. Time-to-Digital Converters with an internal clock up to 100 GHz will allow for a precision measurement of an event time on the chip, if the event signal reaches the chip rather undistorted.

5.2. Tasks for testing and interfacing RSFQ circuits

5.2.1. Design-for-test (DFT)

Ultra high-speed circuits must be designed with system and testing aspects in mind to allow for checking the dc parameters and the functionality of essential sub-circuits at the specified clock frequency. In addition to the specified input and output lines auxiliary high- and low-speed lines should be provided in the layout at the chip level, especially during the development phase to locate conceptional and technological errors by measurements.

DFT is required for developing special test designs for on-chip high speed tests (BIST) with low-speed testers. Fault models and fault diagnostic have to be included in DFT and BIST.

5.2.2. Testing of RSFQ circuits

Testing of HTS and LTS circuits is complementary and will not be described here separately.

5.2.2.1. Built-in-self-test (BIST). Owing to the Josephson relation between frequency and voltage a periodic oscillation and a frequency division on the chip can easily be traced in monitoring the corresponding dc output voltage. Even periodic test sequences of a few bits, generated by ring shaped RSFQ circuits, may be tested in this way.

Bitwise high speed testing comprising a (automatic) test pattern generator (ATPG) and a shift register receiver with a capacity of about 2^{10} bit on the same chip that may be read out at low speed in the MHz range yields useful information on the functionality of digital circuits without ultra-broadband amplifying interfaces. Similar built-in self-tests can be applied if the fabrication technology allows for a sufficiently large circuit complexity.

Here, an example is given for performing a high-speed and on-chip test of the bit-error rate (BER). The class of RSFQ ring circuits provides a unique measuring tool for high-speed digital testing of RSFQ circuits and for the detection of single switching errors. Ring-shaped circuits in RSFQ logic enable the generation and maintenance of permanent SFQ pulse circulation. They are composed of segments of Josephson transmission lines (JTLs) and other RSFQ components [12]. Figs. 21 and 22 illustrate the principle of operation of an RSFQ ring circuit for testing of T-flipflop (TFF) and multiplier (MULT) components. The reliability in circuit operation was proven experimentally by a Bit-Error Rate BER $< 10^{-16}$. The circuit was realized

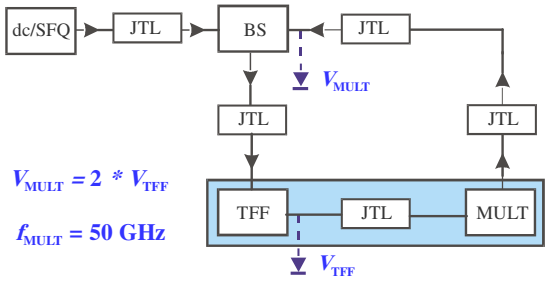


Fig. 21. Testing of RSFQ circuits: ring-shaped RSFQ circuit for Bit-Error Rate (BER) experiments in SIS (Nb/Al_2O_3–Al/Nb) technology, block diagram with dc/SFQ: dc/SFQ converter, JTL: Josephson transmission line, BS: confluence buffer stage, TFF: T-flipflop, MULT: multiplier.

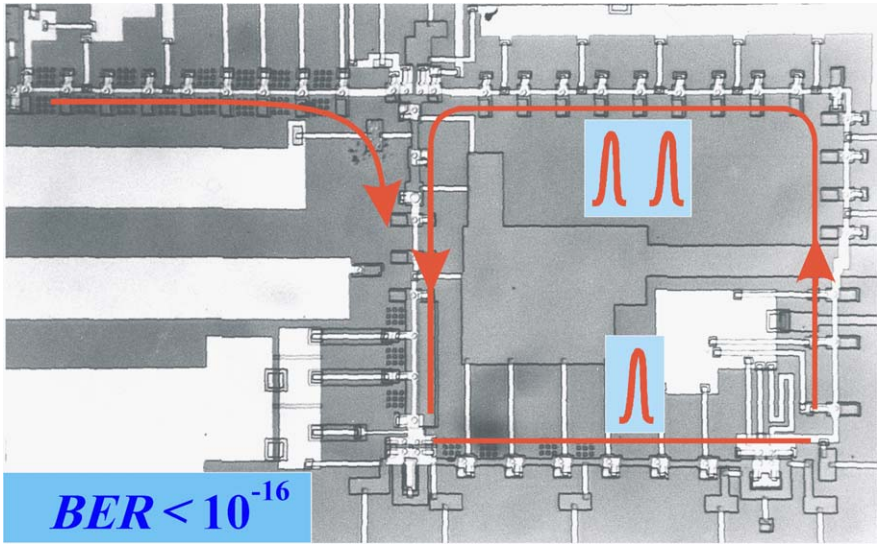


Fig. 22. Microphotograph of the ring-shaped RSFQ circuit for Bit-Error Rate (BER) experiments in SIS (Nb/Al_2O_3–Al/Nb) technology.

in PTB-4 μm SIS (Nb/Al_2O_3–Al/Nb) technology with externally shunted tunnel junctions (critical current density: 1 kA/cm^2, characteristic voltage: 250 μV, Stewart–McCumber parameter: $\leqslant 1$).

5.2.2.2. Test with low-speed input and output of a chip. The test of functionality of digital sub-circuits starts usually with MHz clock frequencies to avoid small signal to noise ratios in broadband interfaces and large circuit complexity for self-tests on the chip. Special circuits, e.g. time to digital converters can operate with an extremely high internal clock frequency and yet with a low speed input and output clock. Low-frequency test are important for development of fault models to support DFT and BIST requirements. Simulations are required for the high-frequency and low-frequency path from the device through the package to the test equipment.

5.2.2.3. Test of superconducting subsystems in a semiconductor environment with high-speed input and output. A subsystem comprises a single chip or several chips with off-chip interconnects and the corresponding module packaging suitable for thermal cycling. The functionality of digital superconducting subsystems must be checked for every bit at the wanted clock frequency up to about 20 GHz for Josephson current density of 1 kA/cm^2. The bit error rates should be determined with available conventional pseudo-random bit sequence generators and receivers with semiconductor electronics at room temperature operating in the Non-Return-to-Zero (NRZ) mode at input and output and requiring input levels within a fraction of 1 V.

High-speed/low-power interfaces are needed to convert the NRZ-mode into the Return-to-Zero (RZ) mode of RSFQ-circuits and vice versa at the output. RSFQ-converters from RZ- to NRZ with the $Nb/A1_2O_3$–Al/Nb technology have already been implemented at the University of Karlsruhe as shown in Fig. 23 [13].

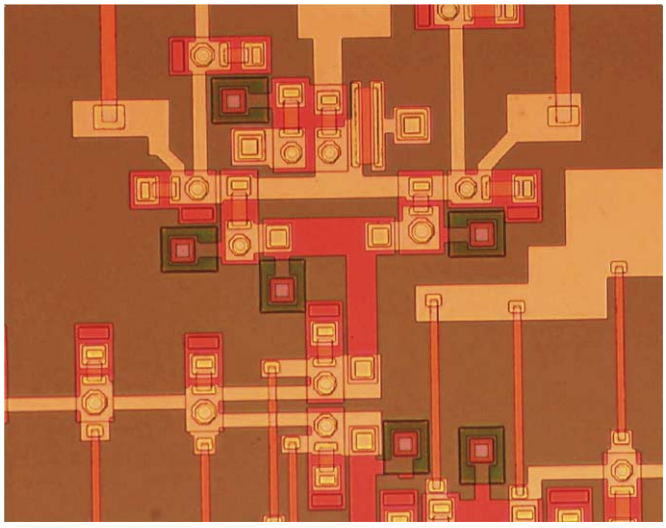


Fig. 23. Micrograph of RZ—to NRZ-RSFQ circuit in the $Nb/A1_2O_3$–Al/Nb technology.

In addition, broad band low noise amplification from the about 200 μV output level of RSFQ circuits is required in several steps: at 4.2 K low noise/low power broad band preamplifiers up to several mV with SQUIDs put in series and controlled by RSFQ circuits and at higher temperatures semiconductor amplifiers. The cut-off frequency of field effect transistors can be roughly doubled in cooling down from 300 K to around 60 K. Moreover, the noise temperature is considerably lower at 60 K than at 300 K. An amplifier hierarchy is chosen to meet the subsystem specifications, e.g. total cooling power, PRBS-rate at the required clock frequency. Additionally, high-frequency, high pin-count probes and test sockets are needed. Appropriate multi-chip modules with superconductive microstrip lines with high bandwidth for hybrid packaging are required. The limits of test issues and test technology are

set by high bandwidth, high direct conversion sampling rates, higher dynamic range, lower noise floor integration of analog, digital test and costs of equipment. One important issue is samplers with a bandwidth of more than 50 GHz and 16-bit resolution.

High-speed optical interfaces must be installed for multi-channel input and output to overcome problems of cooling power, interference and ground noise.

5.2.3. Measurements of technological parameters

The design of RSFQ circuits strongly depends on the reproducibility of the fabrication process. The quality of the fabrication should be controlled semi-automatically by measurements of important parameters on specially designed test areas or test chips: standard deviation σ, spread Δ on a chip, on a wafer and from wafer to wafer. Wafer mapping of key parameters yields enabling information for the fabrication and the circuit design.

Important parameters are:

Josephson current, Josephson current density as a function of junction area,
I_cR_n-product,
junction count in array circuits at microwave propagation by precise voltage metrology,
sheet resistance, sheet inductance (London penetration depth),
defect density due to holes and shorts in insulating layers,
dielectric constant,
losses, surface roughness and planarization quality,
quality of vias between metallization layers.

Understanding the chip failures and providing corrections require the ability to localize faults to an area of the chip that can be inspected. Therefore diagnostic tools have to be used and software for DFT has to be developed for integration of CAD navigation across the layout. Additionally, delayering processes for depackaging are required.

5.2.4. Instrumentation

High-speed testing might be very expensive. A pseudo-random bit-sequence generator and receiver (10 Gb/s, Anritsu, Agilent) may be purchased for several hundred k€. In addition, low noise dc current sources under computer control, low power/high speed interfaces and amplifiers are needed. Moreover, test jigs for chips at low temperature with a frequency bandwidth up to 20 GHz must be carefully designed. Often, at the chip location residual magnetic fields are required to be smaller than 1 μT.

6. Cooling and system aspects

6.1. Cryocoolers

The commercial acceptance of SDE is strongly limited today by the cooling penalty. This penalty is not only related to the cost and system overhead (electrical power consumption, mass, volume) but also to the poor reliability and/or the constraints of integration of the existing coolers. These existing coolers have been developed for specific applications with specifications that are not directly applicable to SDE devices. The cooler requirements for SDE depend on the specific application and on the operating temperature, and as already discussed in Section 2.5. Gifford MacMahon (GM) coolers have been initially developed for cryopumping and are also commonly used today for thermal-shield cooling in MRI helium cryostats. They are reliable (up to 5–8 years of operation with low maintenance), but they have a low thermal efficiency and are relatively massive. Their typical performance range is from a few watt at 10 K up to a few hundred W at 80 K for an electrical input of a few kW. Recently, GM coolers capable of 1 W of cooling power at 4 K have been introduced for helium recondensation or dry magnet cooling. They use rare earth based magnetic materials in the regenerator which may perturbate or be influenced by magnetic fields.

Joule Thomson (JT) expansion of air, nitrogen or argon in open cycle coolers is widely used for IR detectors cooling near 80 K in missile guidance systems. These coolers with low cost and high reliability (because of their technical simplicity) are unfortunately not adapted for continuous and efficient operation (the high feeding pressure required for thermal efficiency is not compatible with simple and reliable compressor technology). The use of appropriate gas mixtures may solve this problem to some extent, and allow for efficient permanent operation in the 80–140 K range of temperature using traditional GM type compression units. For lower cooling temperature (down to 10 K), cascade systems using static sorption compressors are under development for space applications. Their efficiency, reliability and cost effectiveness are not yet proven.

Single stage Stirling coolers, with typical cooling powers up to a few watt in the temperature range 50–80 K, have been widely developed for infrared detectors cooling for military applications. Their high thermal efficiency and small size (due to high operation frequencies—in the range of 50 Hz—determined by pneumatic resonance conditions for the pressure oscillator) are attractive for SDE applications. Their typical MTBF today is unfortunately limited to about 5.000 h due to sliding friction of both pressure oscillator and cold expander pistons. Ongoing developments on surface coatings and gas bearings may increase this MTBF to a few 10.000 h in the future. Specific developments for space applications, using frictionless flexure bearings and clearance seals between pistons and cylinders, have allowed for coolers to be manufactured with lifetimes, without maintenance, over 5 years. The cost of space qualified coolers are unacceptable for SDE applications, but they may probably be drastically reduced for large-scale production. Recently this frictionless flexure bearing technology has been introduced in commercial Stirling coolers for IR detectors cooling (see Fig. 24). Significant cost

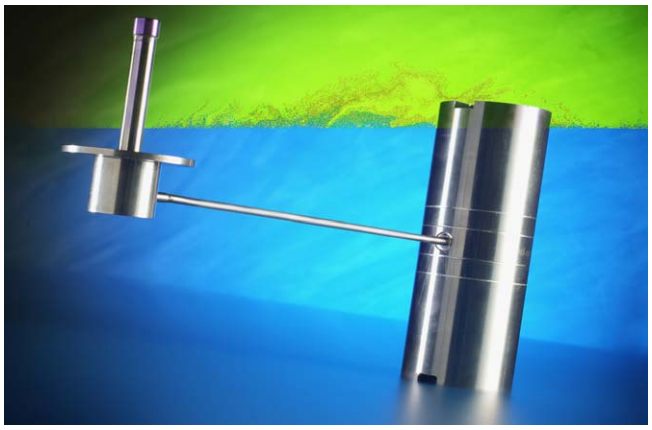


Fig. 24. 1–3 W at 80 K Flexure Bearing Stirling Cooler (Courtesy of THALES).

reduction should be obtained compared with space coolers with long MTBF preserved.

The Stirling coolers for space applications have also been developed in two stage versions for a few 100 mW of cooling down to 10 K. Single stage cooler with improved regenerators could also be capable of cooling in the 20–30 K temperature range of interest for MgB_2. They have also been coupled to JT expansion loops, allowing for a few mW of cooling at 4 K.

A new concept of cooler is now emerging: the pulse tube (PT). Basically, a PT is operated like either a GM or a Stirling cycle. Its main feature is that any mechanical moving part has disappeared in the cold expander: the cycle helium gas itself acts as the mechanical expander of the traditional Stirling or GM coolers. The phase shift between pressure and mass flow oscillation amplitudes (required to get the cooling effect) is pneumatically controlled by passive components (surge volume, flow impedances). The advantages of this absence of moving parts in the cold expander are evidently manyfold:

- simplicity of manufacturing the expander (low cost),
- reliability (long life),
- simplicity of integration,
- reduced disturbance (piston vibrations, motor electromagnetic signature).

Recent developments on PT coolers have demonstrated that their thermal efficiency may be practically equivalent to that of Stirling coolers. One of the major interests of the PT concept for SDE applications is the possibility to design and integrate the cold part of the PT simultaneously with the design of the SDE device, allowing for a better packaging. Efficient PTs have already been developed for space applications driven by long life time flexure bearings compressors. Cooling powers of 1–7 W at 80 K have been demonstrated with different prototypes.

GM type PT's use the compression units of commercial GM coolers directly. The pressure wave in the pulse tube is established by a separate valve unit. Stirling type PT's require some adaptation of existing pressure oscillators (resonance conditions). The reliability development effort is now restricted to the pressure oscillator since the cold expander (which is also a critical component for traditional Stirling coolers) no longer has a moving part. A two-stage 4 K PT is now commercially available (see Fig. 25) driven by a 5 kW compressor with 0.5 W at 4.5 K and 40 W at 50 K available cooling power. Single stage PT prototypes have also demonstrated cooling powers in the range of 35–100 W at 80 K (see Fig. 26).

The PT concept is potentially a promising opportunity to solve the traditional cooling penalties if its integration is taken into account at the very beginning of the SDE device conception.

The availability of reliable 4 K mechanical coolers has also lead to the recent development of mechanical subKel-

Fig. 25. 4 K Pulse Tube Cooler (Courtesy of CRYOMECH).

Fig. 26. 80 K Pulse Tube Cooler (Courtesy of AIR LIQUIDE).

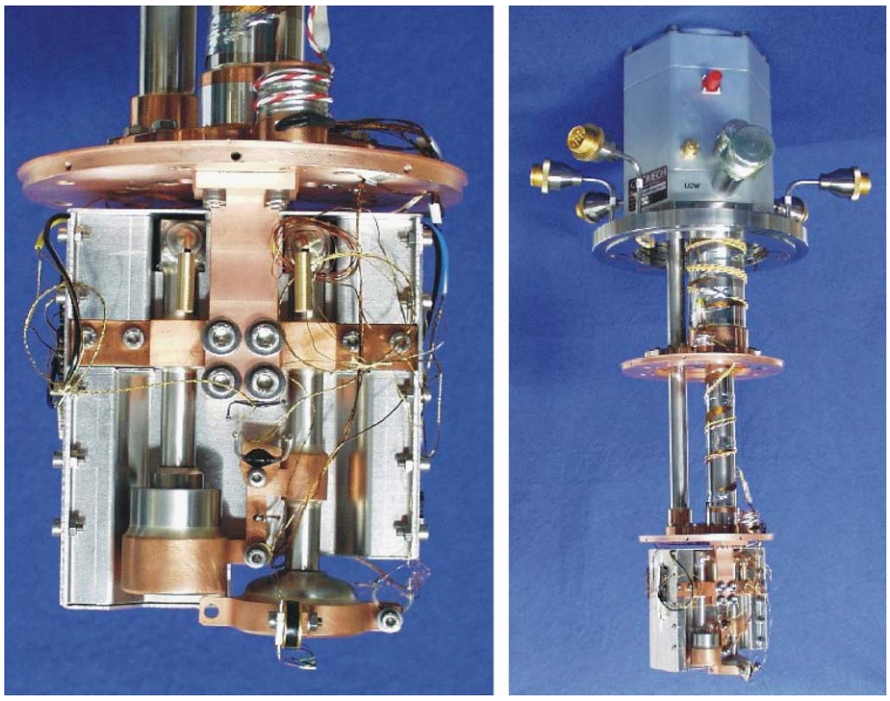


Fig. 27. 300 mK sorption cooler attached to 4 K PT (Courtesy of AIR LIQUIDE).

vin coolers. He3 sorption coolers (300 mK) and adiabatic demagnetisation stages (100 mK) have been coupled to 4 K PTs as precoolers (Fig. 27). The coupling of dilution fridge (50 mK) is under development.

6.2. Trends in cooling

In the developments towards the ideal cooler, during the last few years the cooler requirements seem to have been addressed one by one: high reliability, low cost, and small size.

6.2.1. High reliability

Three to five years ago, the hot issue was reliability. Available coolers had specified lifetimes of the order of one year, whereas the requirement for most civil applications was over 5 years. Developments were on the compressor and on the cold head (the gas-expansion unit). Concerning the latter, main attention has been on eliminating the moving parts in the cold-finger. Typical examples are the pulse tube refrigerator and the developments in Joule–Thomson cooling. With respect to the compressor, the key issue was the rubbing contact between the compressor piston and the cylinder. Wear out of the rubbing seals that were applied was the limiting factor in compressor lifetime. Now, these rubbing contacts can be eliminated by using flexure bearings that support the piston and the displacer inside their respective cylinders without any contact. By very accurate machining the gap between piston and cylinder can be reduced to a few μm. The flow impedance of this clearance gap is so high that it acts as a dynamic seal for the helium gas. Because of the extremely narrow gaps the bearings that support the pistons have to be stiff in the radial direction and weak in the axial direction. This is realized with so-called flexure bearings. The MTTF of these compressors can exceed 50,000 h, whereas standard Stirling compressors have MTTF levels of less than 10,000 h, and more typically 5000 h. The work on these long-life compressors was pioneered by Davey of the University of Oxford in the early and mid-80s. These were developed especially for space applications with extremely long life (10 years) in single pieces and, therefore, at high cost. Nowadays, these compressors are under development for highly reliable long-life pulse tube coolers (mostly for cooling HTS filters) and are also available in some commercial coolers.

6.2.2. Low cost

Another challenge is the realization of these highly reliable coolers at a sufficiently low price. As mentioned in Section 5.1, a price of 10% of the total system cost is generally accepted, but of course the lower the better. Cooler manufacturers are continuously improving the design and manufacturing of the cooler with cost being the main driver. These developments towards lower cost were largely stimulated by the US DARPA program that sponsored research aiming at $ 1000 coolers. Also the production volume is an important cost determining parameter. As a rough indication, the price per cooler goes down by a factor of two when the number of coolers produced is increased by one order of magnitude.

6.2.3. Small size

At present, more and more attention is paid to the size of the cooler. This parameter should also be related to the total system. Again, something like 10% is acceptable. Since devices get smaller and smaller, cooler miniaturization becomes more and more important. Because also the dissipation can be very small (as in most SDE), there is a need for extremely small coolers (order cm) with small cold heads (order mm) and low cooling powers (mW level). Extreme miniaturization is investigated by applying micromechanical techniques.

6.3. Cryopackaging

Packaging of electronic devices, usually, refers to sealing the devices against negative influences from outside (e.g., moisture). This is done by coating the device with a protective layer, or by placing it in a hermetically sealed ceramic package. With respect to superconducting devices, however, packaging also includes the 'cryopackage'. That means that the device, the cooler, and the thermal insulation are considered as a whole, a single package.

The important issue in cryopackaging is the reduction of the thermal load to the device. A higher load means that more input power is needed and a bigger, heavier, and more expensive cooler. Four contributions to this heat load can be distinguished: conductive flow via gas in the vacuum space, conductive flow via the mechanical supports, conductive flow via the data lines, and thermal radiation.

6.3.1. Residual gas in vacuum space

Depending on the system dimensions and the acceptable conductive load, residual gas starts to become relevant above a pressure of roughly 10^{-2} Pa. The problematic gas source in this respect is outgassing. Proper design, clean machining and manufacturing is a prerequisite. Also, extended pumping at an elevated temperature is necessary before operating the cooler in its package. Furthermore, chemically active getters have to be applied in order to obtain vacuum life times of more than a year.

6.3.2. Mechanical supports

The best materials to be used for supports are engineering composites, epoxies reinforced with fibers of glass, carbon, Kevlar, etc. These have a low thermal conductivity combined with a high yield strength. Usually, small composite straps are applied with unidirectional fibers that are loaded under tension.

6.3.3. Data lines

As is the case with material supports, materials should be used that have a low thermal conductivity. Also, the conductive load via the lines can be reduced by increasing their lengths. The optimum configuration, however, is a purely optical coupling. As mentioned in Section 2.3.4 this requires the development of a high-speed optical modulator.

6.3.4. Radiation

Radiative load can be significant. A black surface measuring 10 cm × 10 cm radiates close to 5 W at 300 K! However, polished metallic surfaces can be used with emissivity factors below 0.05, thus reducing the emitted radiation to below 0.25 W for this area. A further reduction of the radiative load is to use a thermal radiation shield. Also, the number of shields can be increased, thus arriving at multi-layer insulation (MLI). Usually, thin aluminized mylar foil is used for this purpose. The disadvantages of MLI are the higher costs (material and labor) and an increase of the out-gassing rate.

6.4. Cooler interference

A special aspect of cryopackaging is the cooler interference, and ways to deal with that. Depending on the specific device application, this interference can be electro-magnetic interference (EMI), mechanical vibrations, and/or temperature fluctuations. EMI can be caused by currents running through the compressor coils or the motors that drive the valves or the displacer, and by moving magnetic material. Mechanical vibrations are caused by the movement of pistons, displacers and valves. Also, a gas flow or pressure oscillations may cause mechanical vibrations. The cold-tip temperature may fluctuate with a characteristic frequency (in regenerative coolers the operating frequency). Besides the oscillations, also a low-frequency drift in temperature is possible.

By far the largest part of the noise that a cooler is generating arises from moving parts. These parts are in some way driven by motors with current-carrying coils that generate EMI and also vibrations result. Therefore, the elimination of moving parts in the cold stage results in low-noise cold heads, as for instance in the case in JT-coolers and pulse tube refrigerators. Furthermore, non-magnetic or even non-metallic components should be used in order to reduce EMI. It is obvious that, besides the cold heads, it is also attractive to develop compressors without moving parts. The main effort in this respect is on sorption compressors.

The most simple approach for the suppression of cooler interference is to switch off the cooler at the moment the superconducting device is to be used. There are two problems in time separation: firstly, the cooler should not be switched off too frequently because that will seriously limit its lifetime, and secondly, the temperature of the device will slowly increase (thermal drift). Both problems can be solved by incorporating a sufficiently large thermal buffer: a thermal storage unit. To stabilize the temperature it is best to apply a buffer with a phase change material involved (e.g., a boiling liquid).

Besides separation in time, cooler and device can also be separated in space. The problem to be solved in the case of space separation is how to transport the heat from the superconducting device to the cooler. Three possible interfaces can be conceived: a heat pipe, a forced gas circulation and a thermal strap.

7. New devices and materials

7.1. New concepts for superconducting devices

7.1.1. Introduction

Several concepts for new and exciting superconducting devices have emerged in the last years. These result, for example, from groundbreaking advancements in basic research, such as the identification of the unconventional symmetry of the superconducting charge carrier system in the high-T_c cuprates, new materials, like magnesium diboride and the organic superconductors that were recently discovered, or from novel ways to control material properties, such as field effect doping and intercalation. Fabrication procedures continue to advance considerably, creating opportunities for novel devices. For example, Al-based superconducting qu-bits can be fabricated with interestingly long decoherence times. Similarly, impressive progress has been achieved in the precise control of heterostructure growth. Barriers of tunnel junctions are designed and fabricated with unprecedented precision, opening the route to promising devices such as non-hysteretic SINIS junctions, or junctions with ferromagnetic barriers characterized by a π-shift of the order parameter phase. Especially important are developments in film growth which were initiated by high-T_c superconductivity. Based on this progress, a wide spectrum of functional materials, in particular oxides, can now be combined into heterostructure devices, opening up a new field of oxide electronics. These advancements offer possibilities to enhance device performance, to create new functionality or to design new circuits. This progress seems to continue and to not slow down in the future.

7.1.2. Enhanced performance in established structures

Demands on junctions depend upon the type of applications. A high characteristic Josephson voltage, i.e. a high I_cR_n product (where I_c is the Josephson critical current and R_n the normal state resistance of the junction), is needed for high frequency and high speed operation as well as for low noise. High-T_c superconductors should, in principle, be able to give a large I_cR_n product, but nodes in the gap of the d-wave symmetry may decrease the product considerably. For stable operation, a non-hysteretic I–V behavior of the junctions is needed. This is usually obtained by external resistive shunting. Again, however, high-T_c superconductors are of advantage because of inherent shunting due to the nodes in the d-wave energy gap. Limitations in circuit inductances put limits on the maximum critical current of a Josephson junction while thermal noise limits it minimal value. Integrated digital electronics demands a high degree of reproducibility and uniformity between large numbers of junctions, both on and between chips. A sharp rise in the I–V characteristic at the gap voltage may be advantageous for the conversion gain and noise of an SIS low noise mixer while the gap value puts a limit to the highest frequency that can be converted. Bolometers and mixers that are biased at the superconducting transition point also need a sharp transition. A compromise between, for example, cost of refrigeration, thermal noise, frequency, and integration possibility may imply that a material that has not the highest T_c may still be the most suitable choice.

7.1.2.1. Enhanced I_cR_n-products. The I_cR_n product determines the high frequency limit/speed and the amplitude of the output signal for the Josephson junctions. Depending on the way J_c is altered, it may be proportional to J_c^n, where n varies between 0.4 and 0.7. An obvious way to increase the frequency limit is to increase J_c. High I_cR_n can be reached in principle using high-T_c material. Values of 8 and 10 mV at 4 K were reached, respectively, using 24° [1 0 0]-tilt boundary bicrystal junctions or ramp type Josephson junctions. These results indicate that circuit operation up to 5 THz can be achieved if other circuit demands are met.

7.1.2.2. Sub-micron junctions and transmission lines. Submicron size lines and junctions may be of advantage in HTS components and circuits. The power in J_c dependence of the I_cR_n product leads to a high critical current density which, in turn, implies that the junction area has to be kept small to avoid too large values of I_c or too small values of R_n to match the circuit environment. The flow of vortices may be impeded by the boundaries of the lines. A grain boundary is inhomogeneous in several length scales and some disturbing defects may be avoided by using small dimensions. However, small line widths also imply that the defect rich boundary regions become more dominating.

Si-CMOS devices have reached linewidths of about 130 nm for the device critical size. The roadmap of Si-CMOS predicts that the 100 nm limit will be reached in a few years in production. A much smaller effort has been invested in the development of superconducting submicron technology.

SQUIDs and SFQ circuits require that the critical current and the inductance of a circuit loop with a weak link are limited, so that their product equals about a flux quantum ($I_cL \approx \Phi_0$). As it is hard to fabricate a loop with a low inductance, the critical current should not exceed a few tens to a few hundred μA (at the same time the Josephson coupling energy, i.e. the critical current, should surpass the thermal noise energy). To fulfill this demand, junctions with sub-micron size are required. Bicrystal and ramp HTS junctions with widths down to 200 nm have been developed. More work is needed to obtain spreads in junction parameters that will allow integrated circuit fabrication. Naturally, once the sub-micron technology is developed, sub-micron transmission lines can be employed. Recent progress in this direction, designing, fabricating nanolines and testing at 16 GHz has been achieved in cooperation of the PTB Braunschweig and the University of Karlsruhe [14], see Fig. 28.

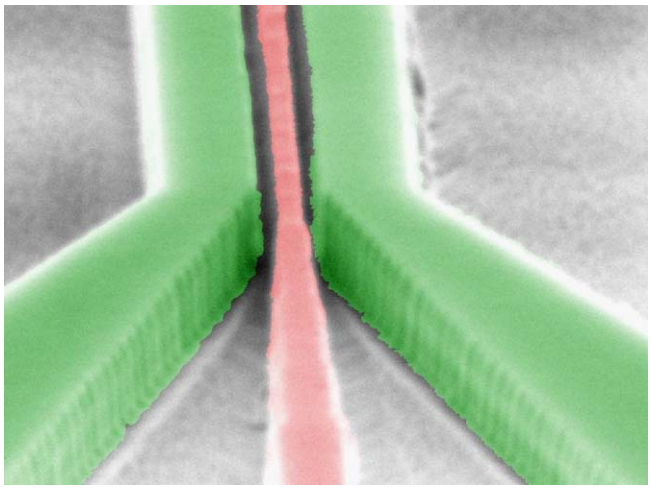


Fig. 28. SEM micrograph of a coplanar waveguide of Nb on an oxidized Si-wafer fabricated at PTB Braunschweig. The inner line width is about 100 nm, the length is 3.2 mm.

Sub-micron Josephson junctions are needed for very small superconducting integrated circuits that can function in a frequency range of several hundred GHz.

7.1.2.3. Non-hysteretic junctions. Most of the applications in digital and analog superconducting electronics require Josephson junctions with non-hysteretic I–V curves. In conventional, low temperature superconductors (LTS), non-hysteretic I–V characteristics are achieved by adding an external resistive shunt to the junction. The external shunting results, in practice, in large junction size, low characteristic Josephson voltages, and makes sub-micron- and nanometer Josephson devices less attractive.

LTS Josephson junctions with non-hysteretic characteristics can be developed if critical current densities of 10^5 A/cm^2 are achieved. This implies that the thickness of the oxide layers should not exceed one or two atomic layers. Several groups in USA have reported critical current densities of this order for a small number of devices but with low reproducibility. In Europe, the group at PTB, Braunschweig can challenge these results. Obviously, to achieve a low spread in device parameters, the control of the oxide layer requires an accuracy of less than one atomic layer—a very demanding task.

An alternate way to obtain non-hysteretic LTS Josephson junctions was recently applied to extreme complex circuits by the PTB group, namely junctions having a barrier which consists of normal metal covered with thin oxide layers from both sides, so called SINIS junctions. The junctions show excellent behavior and reproducibility, however the values of the characteristic Josephson voltage do not exceed ~100 μV. Preliminary results from the same group indicate that values of 500 μV can be reached which will make it possible to work up to 250 GHz. This direction should be further explored in terms of material science and theory in order to determine the upper limit of the Josephson voltage.

HTS Josephson junctions have the big advantage of being intrinsically shunted. This makes these devices excellent candidates for integrated circuits working above 20 K.

7.1.2.4. Intrinsic tunnel junctions in layered cuprates. The cuprate superconductors are characterized by their layered structure. Sheets of superconducting copper-oxide layers are Josephson coupled. In principle, it is possible to etch small columns into single crystals or epitaxial films of anisotropic HTS, and such a column will form an array of series coupled junctions. Beautiful tunneling curves have been registered in such intrinsic tunnel junctions that contained a few, maybe even one, double cuprate layers, stacked in the crystal c-direction. The coupling between layers, however, is weak and the Josephson current is limited (up to about 10^4 A/cm^2) in the junctions that are hysteretic. Single electron tunneling effects may occur. It has been shown that intrinsic junctions respond to microwave radiation up to high frequency and electromagnetic resonances can be seen in I–V (and conductance) curves. The distance between cuprate layers, and the Josephson coupling, can be varied by intercalation and it remains to be shown that a similar procedure can produce non-hysteretic I–V curves. In principle, it may be possible to fabricate integrated circuits using intrinsic junctions but these should preferably be made in epitaxial HTS films.

7.1.2.5. Interface doping. The electronic properties of the high-T_c superconductors resemble in several aspects those of strongly doped semiconductors. The high-T_c superconductors are characterized, for example, by non-vanishing electrical screening lengths, which are utilized in electric field effect devices. Because of the large electric screening lengths, doping can be used to optimize HTS devices. This tool is not available for conventional superconductors, which usually are canonical metals. Doping offers a huge parameter space for device optimization, as the dopant elements, concentrations and profiles can readily be altered. Doping has been proven to be highly successful to optimize the properties of interfaces, in particular of grain boundaries. The most significant of these has been the recent introduction of doping heterostructures to enhance the boundaries' critical current densities without lowering the T_c of the bulk material. By the same token, doping can be used to adjust R_n or the I_cR_n product of grain boundary junctions. Whereas most doping studies have focussed up to now on grain boundary junctions, the same physics seems to apply to other Josephson junctions in high-T_c superconductors as well, offering the same opportunities for their optimization.

7.1.3. New materials and functions

7.1.3.1. New materials. Newly discovered superconductors may offer possibilities of creating novel electronic devices and to improve properties of the existing ones.

(1) *Magnesium diboride, MgB_2 (see also Section 7.2):* MgB_2 is a newly discovered non-oxide superconductor with a T_c of 39 K. Main properties of MgB_2 were mapped within the first six months after its discovery. It is established that MgB_2 is a BCS type superconductor with a coherence length of about 4 nm and a London penetration length of about 10 nm. There are indications of double energy gaps. It has been claimed that this material can become the cornerstone in the development of future superconducting digital circuits working at 20 K, a temperature range that can be reached without expensive two stage coolers (one has previously proposed NbN superconducting circuits that possibly would operate at about 10 K, still achievable with mechanical refrigerators). Films of high quality are ex situ grown on a variety of substrates, including Si and sapphire. Low noise SQUIDs of bulk MgB_2 and thin film SQUIDs with Dayem type nanobridges have been reported. Aiming at electronic integrated circuits, it is obvious that the next steps should be in situ growth of MgB_2 films, their integration in multilayer structures, and the development of reliable Josephson junctions. To reach these goals, basic studies on material thermodynamics and interfaces to other materials need to be performed. The main action in the field is taken by Universities and National Labs in USA and Japan. The research in Europe is driven with limited resources by several universities.

(2) *Organic superconductors*: The discovery of superconductivity in organic materials, such as the so called Bechgaard salts caused great interest. Further, doping of C_{60} films with alkali atoms led to superconductivity at the few Kelvin level; the films deteriorate however rapidly at contact with air. A group at Bell Labs showed that it was possible to dope thin C_{60} films with the electric field effect. They reached $T_c = 52$ K in a hole doped pure C_{60} film at a gate voltage providing about 3 holes per C_{60} molecule. Extending the C_{60} lattice by the insertion of $CHBr_3$, it was even possible to reach a temperature as high as 117 K by field effect. The same group demonstrated field effect superconductivity in benzene like pentazene, tetrazene, and anthracene at the few K level and in polymer films as well. As the electric field can be modulated locally by the shape of gate electrodes, it is possible, in principle, to fabricate superconducting components and circuits. This exciting possibility is discussed below.

The conducting properties of carbon nanotubes are being investigated—metallic, semiconducting, or insulating behavior depend upon chirality (i.e. the folding of the nanotubes) and the number of layers that build up the tubes. Superconductivity has been reported in ropes of a couple of hundred single wall nanotubes (SWNT) that were soldered to Al_2O_3/Pt/Au contacts to give low contact resistance and sample resistance below 10 kΩ. A resistance drop of 2 orders in magnitude was registered below 0.55 K in one of the samples. Proximity induced superconductivity in carbon nanotubes due to superconducting contacts has previously been claimed by the same French/Russian group. Superconductivity (partial changes in susceptibility and resistance) has also been traced below 15 K in 4 Å SWNT in impregnated zeolite. The possible superconductivity agrees with theoretical predictions that T_c is proportional to the inverse of the nanotube diameter. One has to reproduce the results and better understand under which conditions the reported superconductivity exists and how to control the possible fabrication of nanotube components and circuits.

7.1.3.2. π-junctions. One of the unique strengths of superconductivity is the fact that the coherence and the phase of the superconductor's macroscopic wave function can be used for devices. Magnetically induced shifts of the phases are exploited, for example, in SQUIDs used for magnetometry, but phase shifts are also of interest for quantum computation or for the realization of the complementary SQUID technology, as proposed by a group at Stanford. Here, besides the conventional Josephson junction, a new family of Josephson junctions characterized by a π-phase shift across the junctions, so called π-junctions, is employed. The feasibility of such π-junctions was recently demonstrated by a group in Augsburg in the form of a fully epitaxial dc π-SQUID, exhibiting excellent performance. This device is based on high-T_c grain boundary junctions induced by tetracrystalline substrates. A novel biepitaxial technology has been advanced by a group in Naples. It allows the fabrication of more complex π-circuits. The Twente group has very successfully demonstrated another new approach to fabricate π-junctions by using ramp Josephson junctions connecting low-T_c and high-T_c superconductors. Researchers at Chernogolovka, Twente, and Leiden have developed Nb-junctions with ferromagnetic barriers, resulting in all low-T_c π-junctions. Implications of these devices on the development of electronic circuits with novel or enhanced performance are discussed in Section 7.3.

7.1.3.3. Three terminal devices. Interest in superconducting three-terminal devices is based on several enticing features. A superconducting source-to-drain, DS-channel, a virtually loss-free on-state of the transistor, high current density and low voltage levels are properties advantageous in transistor applications. Furthermore, the possibility of electronically tuning resonance frequencies and propagation velocities in superconducting structures offers attractive opportunities in the design of microwave components like filters, transmission lines and phase shifters. In addition, superconducting transistors are compatible with other superconducting components such as high speed switches, sensors or receivers, and in some cases may even be required to interface such components with semiconducting electronics.

Several types of superconducting three-terminal devices are conceivable and have been fabricated. In general, they consist of a Josephson junction or of a DS-channel, which in some devices has been optimized by the addition of

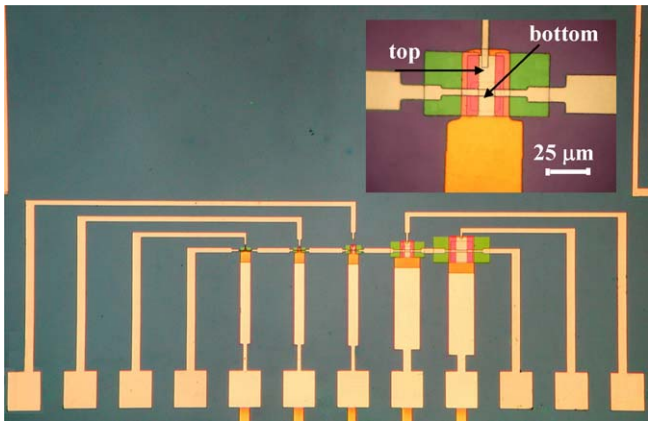


Fig. 29. Nb/AlO$_x$/Nb–Al/AlO$_x$/Nb quasiparticle trapping transistor device fabricated at CNR-IC foundry (Naples).

Josephson junctions. The output of the device is controlled by the application of electric or magnetic fields, or by the injection of quasiparticles into the junction or into the channel. In some cases, the input signal is used to alter the electronic environment of the channel. Three-terminal devices are realized both with low-T_c and with high-T_c superconductors.

The development of low-T_c devices is progressing steadily, and new concepts are continuously being explored. Here, the quasiparticle trapping transistor, proposed by a Oxford–Harvard collaboration and developed by a Naples–Oxford team is particularly valuable, see the device shown in Fig. 29. With observed current gains as high as 70 and signal power gains of 1000, these devices are of interest for measurements and in detection systems.

There are also significant efforts devoted to improving three-terminal devices based on high-T_c superconductors. Their small carrier densities, short coherence lengths, large gap voltages, and high operating temperatures offer advantages for several device concepts, such as superconducting field-effect transistors (FETs).

The superconducting FET is controlled by an electric field, generated either by a ferroelectric gate insulator or by a gate voltage. The electric field modifies the carrier density in the DS-channel, altering the T_c and J_c of the channel. It is possible to tune the T_c of a bicrystal Josephson junction by 10 K. Sufficient depletion of the high-T_c cuprate in the DS-channel induces a phase transition into the insulating, antiferromagnetic state. It has been pointed out by a group at IBM in Yorktown Heights that even for operation at 300 K, this phase transition offers advantages in cuprate FETs as compared to silicon MOSFETs as a means to overcome fundamental length limitations being encountered with the miniaturization of silicon devices. Moreover, FETs built from carbon-based superconductors are expected to show large T_c shifts.

The recent work at Bell Labs on field effect superconductivity in organic films is of great interest. Undoped films of C_{60} could be made superconducting by applying a voltage to a gate to induce charges—electrons or holes in the C_{60} layer. A T_c as high as 52 K was reported for a hole doped C_{60} film and the transition point can be increased to as much as 117 K by expanding the lattice of the C_{60} film by alloying. Lower transition temperatures were obtained with films of a polymer and simple organic benzene like structures. By patterning the gate, it is possible to vary the charge density and form lateral tunnel junctions. The work has only been started and much development is needed to further explore, and optimize, field effect devices of this kind. The reproducibility, stability and noise properties of the devices have to be explored.

The superconducting order parameter of the DS-channel can be modulated by the injection of a quasiparticle current. The performance of these quasiparticle-injection transistors may be strongly enhanced by polarizing the quasiparticles through the use of suitable materials, e.g. semi-metals, for the injector electrodes. This topic is intensively investigated in Japan, in the US, and in Europe at the University of Birmingham. Recent analysis of the experimental data indicates that still there is no experimental proof of this conception. Refined experiments are needed to prove or disprove the idea.

A third possibility to affect the transport in a three terminal device is by the application of a magnetic field. The transport of vortices across a superconducting film or a Josephson junction gives rise to a voltage drop and this voltage depends upon the control current giving rise to the magnetic field. The Josephson flux flow transistor (J-FFT) is considered to be advantageous as compared to the Abrikosov version (A-FFT). Gain has been reported but the high frequency behavior and the noise contributions should be better investigated. Both high-T_c and low-T_c devices have been tested but the present activity is rather small. Flux flow oscillators may be integrated as local oscillators in low noise receivers based on SIS "quasiparticle" mixers.

7.1.3.4. Tuned microwave components. High-Q resonators can be realized using superconducting films. They can be used, for example, in low loss microwave filters having very sharp skirts (fall-offs) for mobile phone base stations. The resonance frequency can be controlled by an adjacent film with a high dielectric parameter. Applying a voltage across such a film, the dielectric function is affected to a considerable extent. The center frequency of the resonator can be tuned tens of percent by a voltage of the order of one volt across a 1000 Å thick film of a ferroelectric material.

Tunable microwave components are, thus, based on the nonlinear susceptibility of a dielectric or ferroelectric gate insulator, such as $Ba_xSr_{1-x}TiO_3$ ($0 \leqslant x \leqslant 1$), which can be changed by applying a voltage to the gate. Electronically tuned capacitors, filters, phase shifters and transmission lines have successfully been built. A great problem is the fact that the high frequency loss factor is much larger in a ferroelectric film than in corresponding bulk material. The losses have been decrease 10–100 times by using matching electrodes to the perovskite ferroelectric film

but they should be decreased another factor of about ten in order to be competitive in commercial devices. High frequency properties were mapped to 40 GHz and theoretical estimates give a frequency limit of several Terahertz.

7.1.3.5. Single charge devices. Single electron tunneling devices may become key components as the sizes of microelectronic circuit elements continue to shrink. A few charges, or even a single charge, may be stored in a memory element. As a charge sensor, the single electron transistor (SET) has an unparalleled sensitivity. The application in digital electronics may be far into the future but already now there are attempts to realize standards (current and capacitance) using single charge devices. A drawback, up to now, has been a limited frequency range due to the loading of the environment of the transistor. A novel RF-SET (that is corresponding to an RF-SQUID where the impedance to the environment is matched via a resonator circuit) has recently demonstrated a charge/energy sensitivity only a few times the quantum limit (3×10^{-6}e/$\sqrt{}$Hz corresponding to $<5\,h/2\pi$) [15]. Even more important, these RF-SETs are fast, allowing sensitive measurements in real time, for example, for the read-out of charge of a charge defined qu-bit [16]. Although these devices do not *need* superconductivity for their operation, their properties are usually enhanced by the metals being superconductors and the interplay between charging and Josephson energies gives an additional degree of device control. In particular, at sufficiently large Josephson coupling such electrometers can operate in the regime of modulation of supercurrent. Due to elastic tunneling of Cooper pairs in this device the zero power dissipates in the electrometer island that is especially important for application in readout of quantum-coherent circuits like Josephson qubit [17].

SET circuits are presently based on the low-T_c Al as junctions can be fabricated in a very controlled way. A superconductor with a larger superconducting energy gap will improve SET performance and, in particular, the decoherence time in qu-bits for quantum computing, see next section. Small Nb tunnel junctions are natural choices and significant effort should be invested in developing Nb technology to the level that it can be used in SET circuits. Some progress in fabrication of small Nb junctions and SET transistors with nominal value of the energy gap of 1.3–1.4 meV and very low subgap current was recently made (see Fig. 30) [18].

SET devices in HTS forms a special challenge because of the unconventional order parameter. Recently, an HTS SET device was fabricated. However, the reproducibility is still at the level at which only single devices can be produced with great difficulty. Another interesting possibility consists in fabrication of stacked arrays of intrinsic Josephson junctions of a HTS crystal [19]. At sufficiently small lateral dimensions of such stack the interaction of Josephson and Coulomb couplings may lead to peculiar transport of Cooper pairs through the stack.

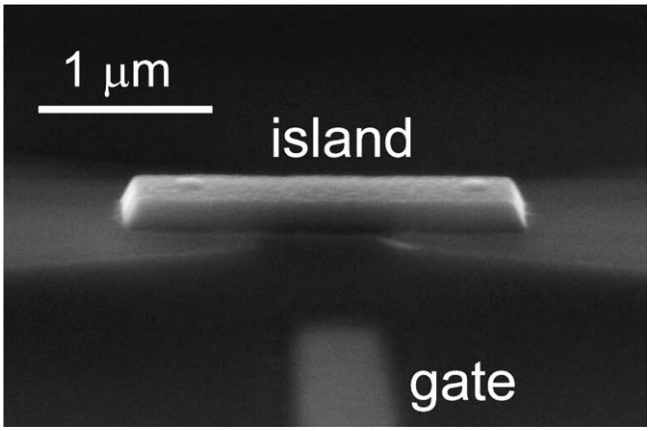


Fig. 30. SEM image of Nb SET transistor with junctions 80 nm by 80 nm fabricated from Nb/Al/AlO_x/Nb sandwich with critical current density $J_c = 1$ kA/cm^2 by chemical–mechanical polishing method [18]. The charging energy associated with total capacitance of the island in this sample is about 50 μeV, that is sufficient for operating in the Josephson charge qubit regime.

7.1.4. New circuits

7.1.4.1. Complementary Josephson logics. A novel approach to superconducting electronics has been proposed on theoretical grounds by a group at Stanford University. The key issue in this novel concept is to make use of SQUIDs that are characterized by transport properties complementary to their standard behavior. In analogy with semiconducting CMOS technology, this concept is called Complementary Josephson junction electronics (CCJ). CCJ-logic combines the speed and low power-consumption of Josephson junctions with large circuit margins. First estimations give gate switching-times of several picoseconds with a tolerance of 30% for the junction critical currents. The logic cell in this technology is based on combinations of conventional SQUID-loops and complementary ones, both with non-latching Josephson junctions. An elegant way to fabricate the complementary SQUID-loops is by introducing a π-junction in the SQUID loop. The π-junction may be the first example where the novel symmetry properties of high temperature superconductors are exploited positively in an application.

7.1.4.2. Rapid single flux quantum logics. See Section 7.4.

7.1.4.3. Superconducting quantum computing. See Section 7.3.

7.1.5. Summary and conclusions

In summary, significant advancements that have been achieved in recent years in film deposition technologies and the development of new concepts have created a wide range of possibilities for new devices or for improvements of existing ones. Technological improvements have been provided, e.g., by the precise control of junction barriers, or by the combination of functional oxide materials into superconducting heterostructures. This progress in sample

preparation will continue, as fabrication facilities allowing device fabrication with unprecedented precision and freedom are becoming available. Further, radically new concepts have been presented which for example are based on the d-wave order parameter symmetry of high-T_c superconductors, or have been suggested in the context of quantum computation.

The advancements described result in new and better performance, new functionality and new circuits. Being oriented to the future, the potential of these technologies is hard to assess. Some of them are close to realization, such as self shunted junctions, others are far away and a topic of fundamental research, such as quantum computation. Although the future of such applications can hardly be predicted, it is fair to say that exciting possibilities are ahead, the foundations of which need to be explored now.

7.2. MgB_2 devices

The recent discovery of superconductivity in MgB_2 with a T_c of 39 K [20] has raised the possibility of devices based on this material operating at 25 K, a temperature much more attractive for cryocooler based operation than the 4 K needed for conventional LTS devices.

MgB_2 shows strong superconducting coupling through grain boundaries and a predominantly s-wave type superconductivity. The two energy gaps in MgB_2 are 2.7 and 7.2 meV, which would allow for Josephson junction I_cR_n products of the order of 6 mV [21], being attractive for high frequency applications. Compared to HTS materials, MgB_2 should have fewer materials difficulties, such as, for example, those associated with step coverage and via filling introducing extra junctions.

7.2.1. Film deposition

The practical exploitation of MgB_2 will require the deposition of smooth, high quality films. Considerable effort has been expended in the preparation of films with T_c close to the bulk value of 39 K. Films deposited as a precursor (either boron, or magnesium deficient MgB_2) with a subsequent annealing step in a suitable Mg rich environment offer an easier route to MgB_2 films with a near-bulk T_c than direct growth of MgB_2 [22]. However, such films tend to have rather rough surfaces that are likely to preclude their use in multi-layer devices. Furthermore, process routes involving annealing steps may introduce difficulties with stability of barrier layers and obtaining stoichiometric lower layers. If a multilayer device design is to be utilised, then a deposition technique that produces smoother films is required. Direct laser ablation of superconducting MgB_2 films is possible, however, such films tend to exhibit a lower T_c than those grown from a precursor [23]. Films grown by molecular beam epitaxy have shown T_c of 36 K without further annealing stages, albeit with poor crystallinity [24]. Arguably, the most encouraging film growth results have come from Penn State group's high pressure CVD process [25], producing films with T_c in excess of the bulk value. For all routes, preventing unwanted oxidation of the film is an issue and may be an additional factor in the selection of barrier materials for ramp and sandwich type junction geometries.

7.2.2. Junction fabrication

For the reasons outlined above, multi-layer heterostructure junctions require significant development and optimisation of film deposition. Single layer MgB_2 junctions and SQUIDs, however, have already been fabricated either utilising localised ion damage or nanobridges to form the Josephson elements.

A group in the University of Twente have demonstrated a nanobridge based SQUID (Fig. 31) [26], in which a 200 nm thick MgB_2 film was patterned into a washer and slit to give a total inductance of around 60 pH. Two nanobridges of 70 nm width and 150 nm length and thickness were structured using a focused ion beam. The nanobridges show a significant current-superconducting phase relationship similar to that of a Josephson weak-link when the dimensions of the nanobridges are smaller than the London penetration depth. Such a device, therefore, shows a critical current modulation with applied magnetic field (Fig. 32). More recently, the Twente group has realized magnetometer SQUIDs that operate above 35 K with films produced using the high pressure CVD process [27]. The nanobridges in these devices are each contained within a single grain of MgB_2 film, allowing for clean transport and excellent superconducting properties. The noise properties are promising for the use of these devices as MCG sensors.

Another group at Cambridge University have also used a focused ion beam to create all MgB_2 devices. In these devices the FIB is used to mill a narrow (50 nm) trench across the full width of a 2–5 μm track (Fig. 33), leaving

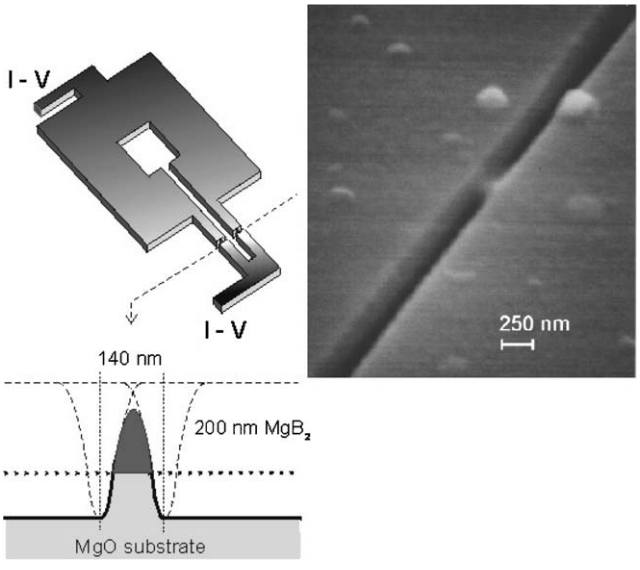


Fig. 31. Schematic and SEM image of a nanobridge MgB_2 SQUID fabricated at Twente.

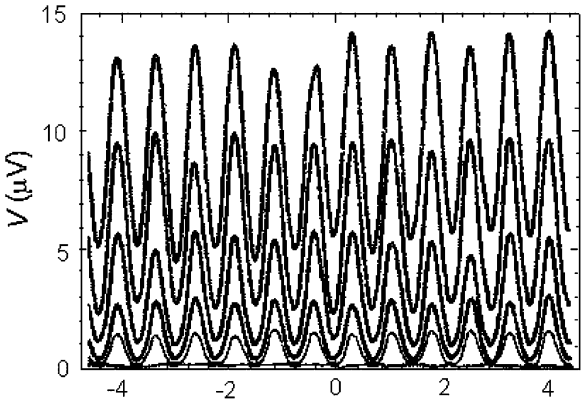


Fig. 32. Voltage–flux modulation curves of the Twente MgB_2 nanobridge SQUID at 15 K at different current biases.

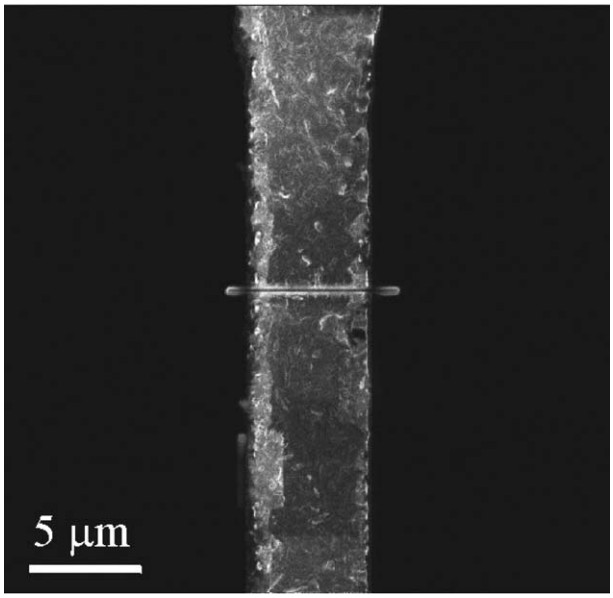


Fig. 33. Focused ion beam microscope image of a MgB_2 SNS junction fabricated at Cambridge University. The track width is 4 μm and the narrow cut is ~50 nm wide.

only 20 nm of Ga implanted MgB_2 in the bottom of the trench. In this geometry, unlike the Twente geometry, there is no nanobridge, however the junctions show both ac and dc Josephson effects (Fig. 34) [28]. From resistance–temperature curves it is apparent that there is a region with a reduced T_c in the junction, resulting from Ga implantation into the bottom of the trench. These junctions are characterised by a relatively high I_cR_n of order 1 mV at 4.2 K which would be very advantageous for high frequency operation.

Using this junction technology, Cambridge have fabricated SQUIDs with a directly coupled pickup loop (Fig. 35) [29]. These devices show very large voltage modulation (>200 μV at 10 K, >30 μV at 20 K) despite having a β_L of approximately 20 (Fig. 36). Initial noise measurements are encouraging, showing a $1/f$ dependency down to 150 Hz and a white noise level of 20 $\mu\Phi_0/Hz^{1/2}$.

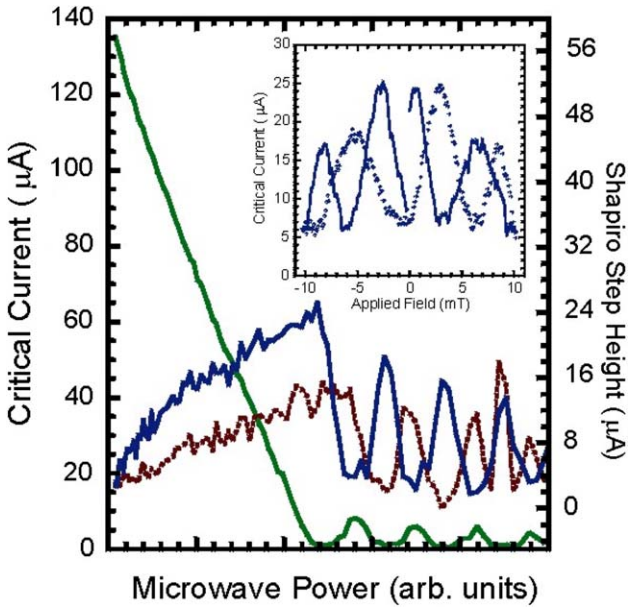


Fig. 34. Critical current versus applied microwave power for a Cambridge FIB MgB_2 junction at 11 K. Inset, the critical current versus applied magnetic field for the same junction at 18 K.

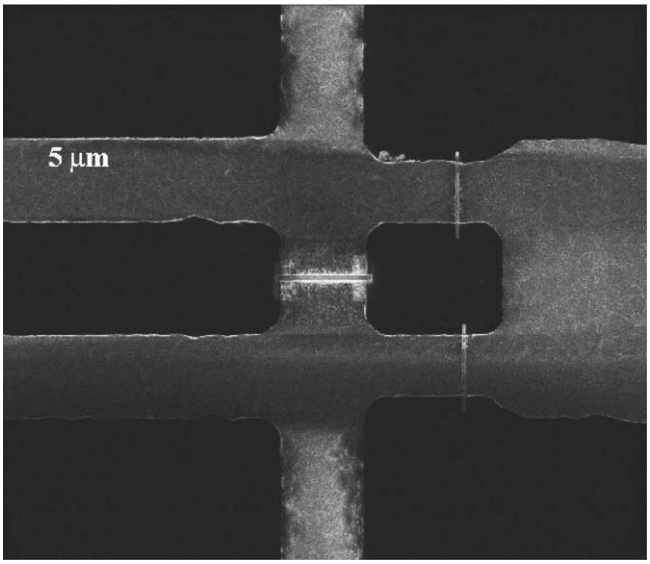


Fig. 35. Focused ion beam image of two FIB MgB_2 junctions in the SQUID loop of a directly coupled pickup loop magnetometer. The track width near the junctions is 3 μm.

Despite the encouraging junction data from these fabrication routes, neither is directly suited to the fabrication of devices with large numbers of junctions as is required to be competitive with LTS and HTS materials. Both techniques involving serial junction fabrication with attendant time and equipment drift issues. The relatively small grain size of the films may also hinder the junction reproducibility, adding further to the difficulties associated with creating reproducible junctions in lateral bridge geometries. This latter problem is most likely to be addressed by the introduction of smoother, possibly epitaxial films of MgB_2.

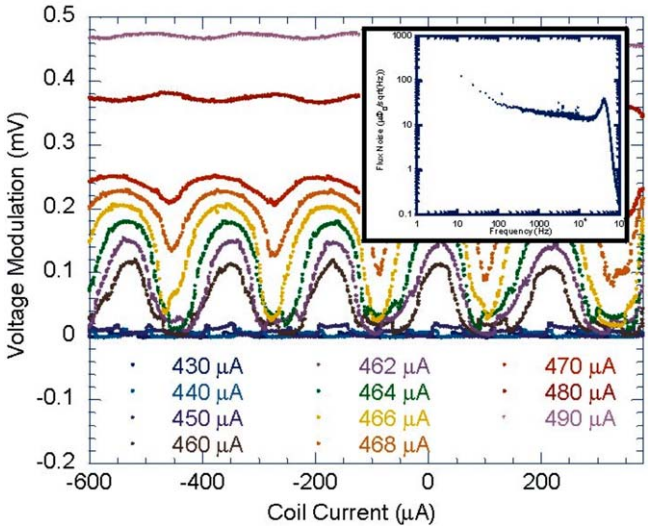


Fig. 36. Voltage–flux modulation curves for the Cambridge FIB MgB_2 SQUID at 10 K. Inset, the noise performance at 20 K.

To overcome the serial fabrication nature, Cambridge are developing a masked ion damage junction fabrication technique. In this route, a thick (450 nm) metal mask is deposited on the film, into which narrow slots (~40 nm wide and 200 nm deep) are milled. The device is then subjected to irradiation by 100 keV H_2^+ ions which are absorbed by the thick metal mask, but pass through the film where the slots in the mask have been milled. After an annealing process the resultant regions of atom-displacement damage create Josephson junctions which show ac and dc Jospehson effects (Fig. 37) [30]. Whilst still at an early stage, these devices demonstrate a potential route for the fabrication of large numbers of junctions, however many issues involving the process protocols and junction uniformity need to be improved.

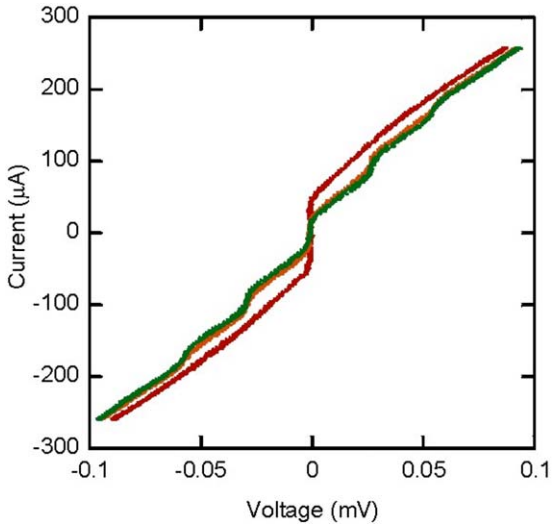


Fig. 37. Current–voltage characteristics with and without applied microwave power for a masked ion damage MgB_2 junction.

Ultimately, the success of MgB_2 devices is dependent on improving the deposition of films. Although the single-layer junctions are useful for investigating numbers of simple circuits, a reliable multilayer process is required for more complex and useful devices, even if it is not required to make good quality junctions. Despite this possibly pessimistic outlook, the scope for MgB_2 devices is large, a preliminary study carried out at Ilmaneau calculating bit error rates due to parameter spread and noise of an MgB_2 device operating at 20 K showed that the error rates would not impose restrictions on reliability and that parameter tolerances would not be unacceptably reduced.

Although many groups are reporting MgB_2 tunnel junctions for spectroscopic purposes, not many groups have succeeded yet in realizing multilayer Josephson junctions with two MgB_2 electrodes. The Twente group developed a ramp junction technology using MgO barriers and MgB_2 counter electrodes [31]. Such a technology, if reliable and reproducible, would truly allow the full exploitation of MgB_2 for superconducting electronics applications.

7.3. Superconductor electronics in quantum computing

The increasing integration density and speed of present day computers is gradually reaching its limiting level. RSFQ circuits may lead to increased speed in a few more generations of computers but radically new concepts may be required, for example employing phenomena of quantum mechanics. Such quantum computers do no longer employ logics based on discrete ones and zeroes but work with a superposition of states that are processed as probabilities in the computation process until read off. Mathematical problems, like factorization of large numbers, encoding and decoding, may be done in a much shorter time than conventionally, opening up new uses. Another large application may be quantum communication and cryptography. So called qu-bits are key elements for quantum computing. A qu-bit is a quantum-system that, similar to a bit in a conventional computer, is characterized by two states, which however can be entangled. Various qu-bit concepts are investigated, based, e.g., on trapped ions, photons trapped in cavities, quantum dots (and interacting ones, ''artificial molecules''), and other single-electron devices.

It is generally accepted that integrated circuits have to be based upon solid state components. The inherent coherency of a superconductor and the relatively large energy separation (the superconducting energy gap) between the ground state and excited states may be of advantage. Very interesting results on such qu-bits have been performed using the charging of a small superconducting island (at NEC [32], at CEA Saclay [33], at Chalmers University [16]) or the circular current flow in SQUID loops (at Delft [34], and at Stony Brook [35]). The charge on the island is a multiple of Cooper pairs, $2ne$, and when an additional charge of only one electron is supplied across a gate, the states with n and $n+1$ pairs on the island become degener-

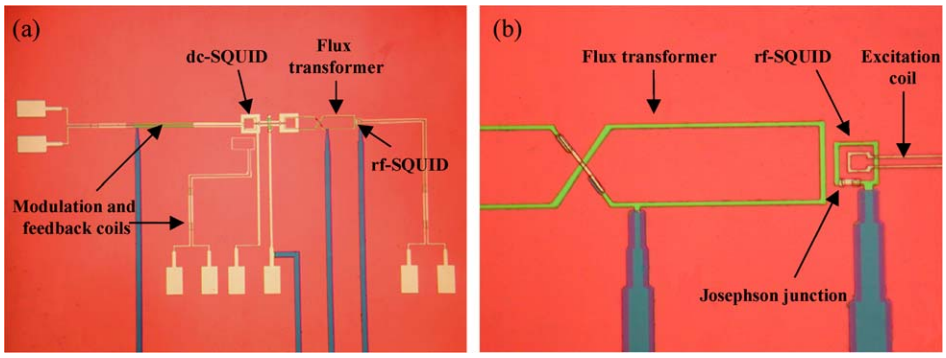


Fig. 38. SQUID based device for macroscopic quantum coherence experiments. The circuit is produced by the Nb/Nb technology available at CNR-IC foundry.

ate and the relatively weak Josephson coupling to the external superconducting electrode mixes them strongly. The macroscopic coherence of superconductors is of great help and the phase of the superconducting wave function may be manipulated. Rabi oscillations in the additional charge were observed and the first successful experiments estimated a decoherence time of ns. Recently, the Saclay group has managed to considerably improve the coherence by better isolating the qu-bit form its environment and reached a decoherence time of 1.5 μs [33]. This was possible due to operating of their qubit (nicknamed Quantronium) in a saddle working point which is in the first order insensitive to external noise. Thorough design of the qubit circuits plays also important role for achieving good quantum coherence characteristics. As example, Fig. 38 shows a SQUID based device for macroscopic coherence experiments.

There are, in principle, two ways that the superconducting junctions may be exploited: in the limits of well defined charge or phase—phase and charge being canonically conjugated variables that are related by basic quantum principles. The macroscopic coherence of SQUID circuits is such an example. Thus, both charge and phase degrees of freedom can be used to process quantum information. Charge and phase qu-bits, having well-defined two quantum states, can each be coupled together to perform two-bit logic operations. Coherence times of the state and the environment, including the coupling to the quantum system, are considered to be crucial factors. At sufficiently weak coupling the coherence times of both superconducting alternatives discussed above have been estimated to be long enough to allow a series of operations before the state is read out. Readout of quantum state can be efficiently realized by applying a switching circuit technique. As a switching element (bistable detector) one can use underdamped single Josephson junction, SQUID or a SET trap. The latter was successfully applied by NEC group for readout of their charge qu-bit [36]. Another approach to the readout problem is based on measurement of reactance (Josephson inductance or Bloch capacitance) of a circuit including qu-bit. Such method is currently applied for qu-bit readout by the TU-Delft [37], Jena [38], PTB [39] and Chalmers University [40] groups. Modification of this method toward realization of non-linear regime (Josephson bifurcation amplifier) was made by Yale University group [41]. For phase qu-bits it is quite natural to use RSFQ electronics for read out and manipulate of the flux state. The EU project RSFQubit which consortium includes the leading European groups working in the fields of digital Josephson electronics and quantum computation addresses these issues. Due to modern technological methods, qu-bits can be integrated on a chip with RSFQ circuits, as well as flip-chip configuration can be used. A great problem is to couple single qu-bits together to perform common operations. It is known that the quantum system is extremely sensitive and delicate. We believe, that without RSFQ electronics this "several qu-bits" problem becomes unless unsolvable, but extremely difficult. Error correction schemes have been proposed to allow for tolerances in the qu-bit performance. These schemes require a considerable increase of the number of qu-bits in a circuit. The investigation of the acceptable qu-bit tolerances are required to evaluate the viability of quantum computation.

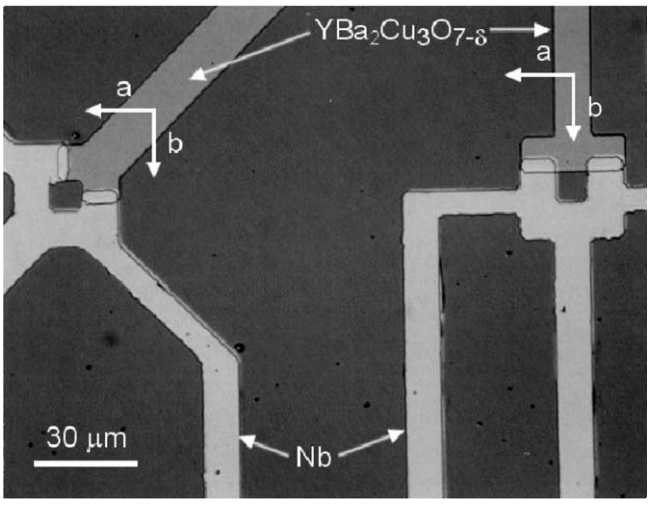


Fig. 39. Micrograph of Nb/YBCO ramp-type SQUIDs. Left: π-SQUID, right: 0-SQUID.

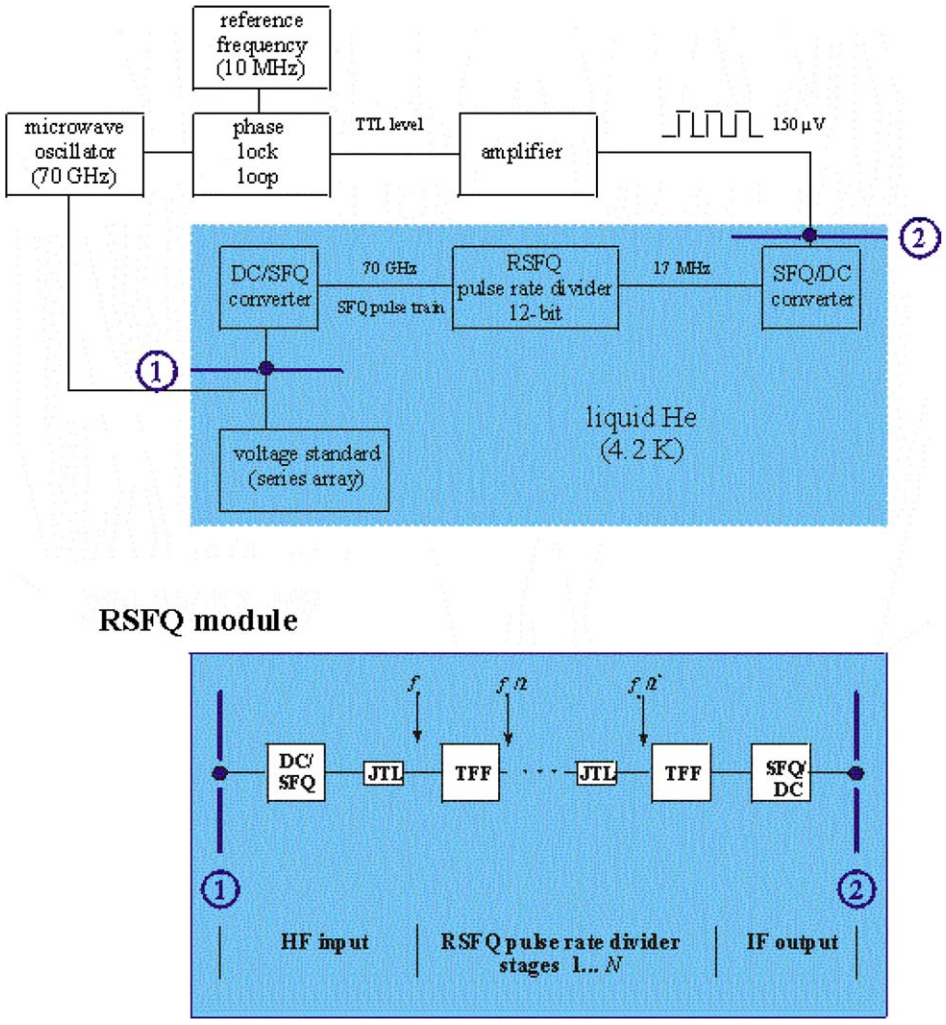


Fig. 40. Josephson voltage standard with integrated RSFQ pulse rate divider.

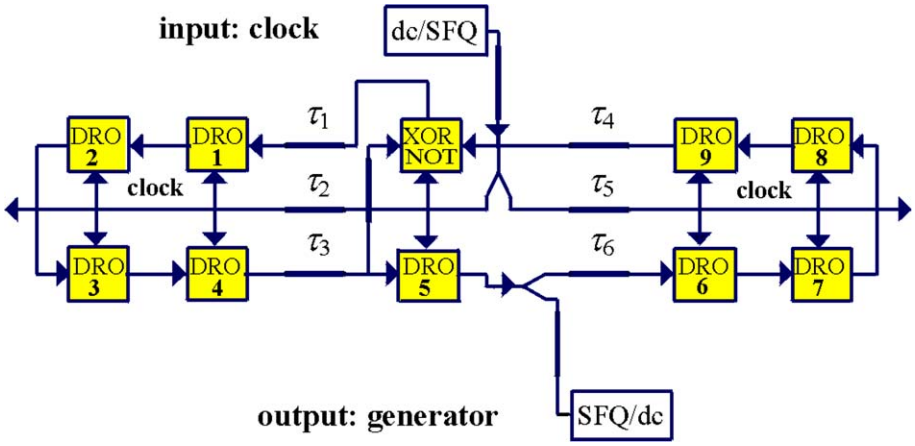


Fig. 41. Pseudo-random noise generator in closed circular pipe line structure. Correct function is achieved for $\tau_4 + \tau_5 > \tau_1 > \tau_2$ and $\tau_2 + \tau_3 > \tau_6 > \tau_5$. τ_4: read-out-/read-in-time for DRO9 and XORNOT, τ_5: propagation time on clock line for clocking of DRO6/DRO9, τ_3: read-out-/read-in-time for DRO4 and DRO5, τ_2: propagation time on clock line between clocking of DRO5/XORNOT and DRO4/DRO1, τ_1: read-out-/read-in-time for XORNOT and DRO1, τ_6: read-out-/read-in-time for DRO5 and DRO6, $(T_P)^{-1}$: maximum clock frequency of the generator, $T_P = \max(\tau_2 + \tau_3, \tau_4 + \tau_5)$.

An upcoming concept is the π-Josephson junction, which in its ground state is biased with a π-phase shift of the superconducting order parameter. This π-phase shift may arise from various causes, e.g. from an unconventional

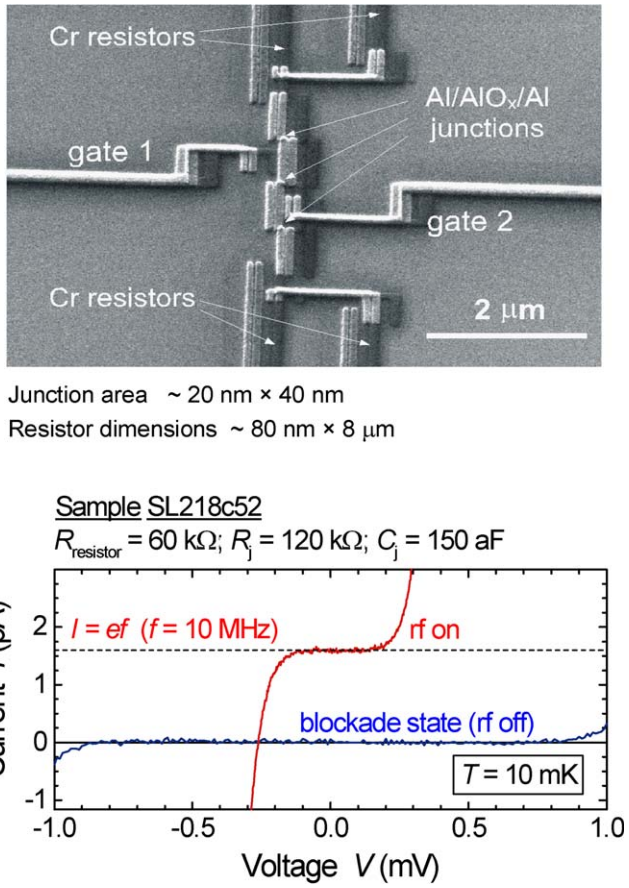


Fig. 42. SEM image (top) and I–V curves (bottom) of three-junction Al–Cr R-pump. The miniature high-ohmic on-chip resistors suppress uncontrolled tunneling (co-tunneling) of electrons across the whole pump and, therefore, make it possible to reduce the number of junctions in the pump array.

order parameter symmetry or from tunneling through magnetic states in the junction barrier. The feasibility of fabricating π-junctions has been demonstrated by various experiments and a dc π-SQUID operating at 77 K was recently demonstrated in Augsburg [42]. Here a tetracrystalline substrate was used. Temperature-controlled crossover from 0- to π-junction as well as an unconventional current-phase relation has been recently reported by Jena group [43]. The π-junction may be the first example where the novel symmetry properties of high temperature superconductors are exploited positively in an application. Recently in Twente π-SQUIDs were fabricated using a thin film technology [44]. Here the base electrode consists of YBCO into which two orthogonal ramps are etched. After resist removal and surface cleaning about 5 nm of YBCO is deposited followed by in-situ Au. Thereafter a counter electrode of Nb is deposited. These junctions may have critical current densities as high as 5 kA/cm^2, at $T = 4.2$ K whereas an I_cR_n-product of 0.5 mV is achieved. The π-shift occurs inside the base electrode in going from the a-axis to the b-axis or vice versa. In the picture below (Fig. 39) a micrograph of a 0-SQUID and a π-SQUID are presented.

Incorporating a ferromagnetic barrier layer between two superconductors also presents a viable means to realize π-junctions. A successful realization of such π-junction circuits was achieved by a Chernogolovka–Leiden–Twente collaboration [45]. More recently, also the integration of superconductor–ferromagnet–superconductor π-junctions and standard junctions on a single chip was achieved [46].

Such π-phase shift devices may be useful in complementary logic [47], in RSFQ logic as bi-stable element and in order to reduce overall bias current [48], in superconducting memories [49], but also as qubit for quantum computational purposes.

Several quantum computing programs have been proposed world-wide lately. The characteristic quantum coherence of a superconductor should not be overseen and the viability of the different schemes based on superconducting electronics should be further investigated and assessed.

It should be remarked that this research is basic in nature, spanning over a larger time than can be foreseen in a roadmap. Scientifically, the field is of great interest, being truly quantum engineering. Technologically, the demand-

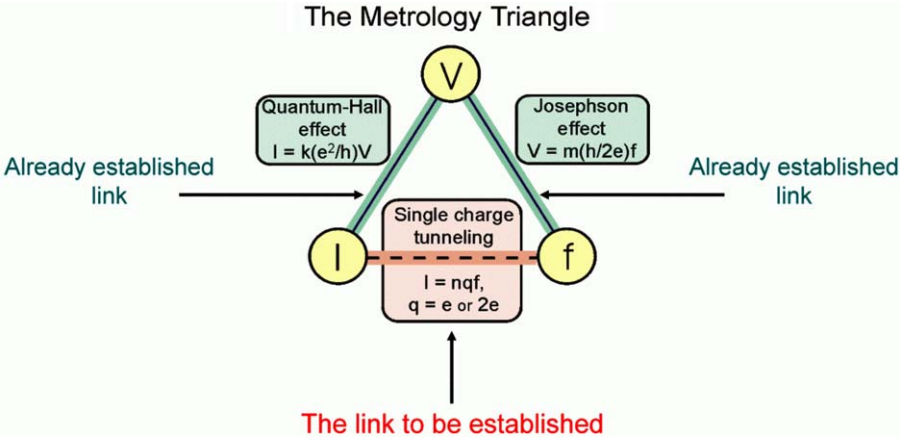


Fig. 43. The fundamental metrology triangle linking basic electrical units and enabling a test of inconsistency of definition of the basic units using three quantum mechanical lows [53].

ing development will have spin-off of benefit to other nanotechnology fields.

In a pilot experiment, the Chalmers group has developed a technique to produce small dots of YBCO film and to make ultrasmall contacts to such a dot. The dots remain superconducting at high temperatures after processing. The produced structures reveal the properties of ultrasmall tunnel junctions, where the YBCO surface layer acts as an insulator. Features typical to the Coulomb blockade of current were observed at low temperatures. The blockade could be periodically lifted under the external electric field. The period of the oscillations was not affected by a magnetic field of up to 5 T, whereas their amplitude went down as the magnetic field was increased. Additional periods were observed that may be interpreted as due to strong electron-electron correlation or non-equilibrium effects. No parity effect was distinguished as yet. The exact reason for this has to be investigated further.

It is important to note that the experiment described above has been the first mesoscopic experiment with HTS materials.

7.4. Superconductor electronics in metrology

The implementation of internally shunted Josephson junctions in both technologies, SINIS and SNS, enables a considerable increase in the circuit integration level (see Section 4). Moreover, they offer common technological bases for realizing new SDE device concepts, and they enable joint integrated circuit architectures including RSFQ circuit modules and large series arrays for programmable Josephson voltage standards [50]. Fig. 40 shows the concept of a Josephson voltage standard under compact frequency stabilization control which consists of Josephson series array with an on-chip integrated RSFQ pulse rate divider. To reproduce voltage values with measurement uncertainties lower than 1×10^{-9}, the frequency of the microwave oscillator must be locked to an adequate stabilized level. At input microwave frequencies of 70 GHz, for proper PLL operation of the device, a 12-bit RSFQ divider module is required to achieve an IF signal frequency of about 17 MHz. The advanced level of SINIS technology-based circuitry, with regard to voltage standard circuits (see Section 2.3.2) and to RSFQ circuits (see Section 4.1.1.1), offers the possibility for dynamic voltage measurements.

For RSFQ logic circuits in LTS implementation, the level of integration reached is high enough for a large variety of digital applications. For signal processing at high frequencies, RSFQ circuit modules can be accommodated on one single chip, which, in turn, offers a variety of digital circuit applications in RF measurement techniques. As an example, to evaluate noise signals, the principle of counting level crossings of band-limited noise signals can be verified by a noise level detector which essentially consists in an SFQ pulse detector of high sensitivity using the dc/SFQ converting principle. Another example is the operation of pseudo-random noise generators. Fig. 41 shows the block diagram of such a device. The generator consists of a 9-bit shift register in feedback operation with an XORNOT gate. It is laid out in closed circular structure and operated in an elastic pipe line mode. In this configuration, the data line of the shift register is folded to a closed circular shape to both sides of the clock line which, in turn, is splitted into two different branches. This results in two simultaneous modes of SFQ pulse propagation in both branches of D-flipflops (DROs), in co-flow (XORNOT, DRO1, DRO2, DRO6, DRO7) and in counter-flow (DRO3, DRO4, DRO5, DRO8, DRO9), respectively. The design allows for an easy increase in the bit length of both branches. For a 20-bit PRNG device operated at a clock frequency of about $f_0 = 20$ GHz, a maximum noise temperature $T_{max} = 30{,}000$ K is estimated. The associated relative uncertainty is estimated at a value of 1.5×10^{-4} (coverage factor $k = 2$, coverage probability of approximately 95%), i.e. slightly lower than for classical noise sources. Such a device may be used as on-chip noise source in real-time digital processing applications.

The metallic nano-circuits comprising small-area tunnel junctions and operating on the principle of Coulomb blockade of single electrons and Cooper pairs are today very important for metrology. The most elucidatory examples are the devices (so-called electron pumps) in which manipulation of individual electrons is performed by applying alternating voltages to the circuit gates. A deterministic current of individual charge carriers flowing through the pump under an rf drive of frequency f, namely $I = ef$ with uncertainty $\sim 10^{-8}$, can be used either for charging the standard capacitance by a well defined number of electrons or be a basis for the electrical current standard. As an example, a three-junction Al electron pump comprising Cr on-chip microresistors is shows in Fig. 42 [51].

Significant improvement of the quantum standard of current, namely a two-order-of-magnitude increase of the picoampere output current seems to be possible by operating the pumps in the superconducting state and transferring Cooper pairs instead of electrons [52]. The advantage of the single Cooper pair devices stems from the phase-coherent properties of the Bose–Einstein condensate leading to resulted in elastic fast transfer of individual pairs. The exploitation of ultra-small junctions made from Nb which critical temperature and, hence, the energy gap, is almost an order of magnitude higher than that of Al can make the circuits more stable against fluctuations and increase the frequency of pumping. The serious problem to be solved in these circuits is a reliable suppression of unwanted quasiparticle tunneling. This tunneling leads to changing of the island parity and operation point.

Increase of the pumping current in single-charge devices up to the level of 1 nA can impact the quantum metrology of electrical units. At this level of current the available cryogenic current comparators enable accurate comparison of currents and closing of the metrology triangle [53,54], shown in Fig. 43.

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